THE pcb design MAGAZINE

April 2014

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MYTHBUSTING

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There are no One-Way Trips!

by Barry Olney, Page 12

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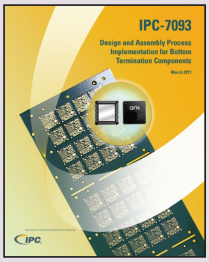

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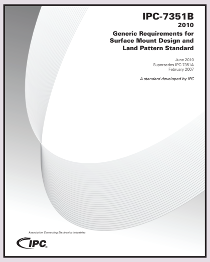

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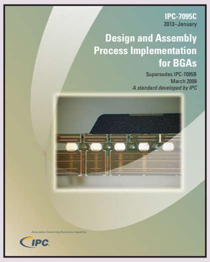

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THE pcb design MAGAZINE™
April 2014

This Issue: MYTHBUSTING

FEATURED CONTENT

PCB designers like to advocate doing the tough work and taking nothing for granted. But there are a myriad of myths floating around in this industry—myths that just won't go away. We face these myths head-on in this issue of *The PCB Design Magazine,* with mythbusting features from Barry Olney, Abby Monaco, and Amit Bahl, as well as articles by Doug Brooks, John Coonrod, and Mark Toth.

FEATURE COLUMNS

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column

THE SHAUGHNESSY REPORT

Out With the Old, In With the New?

by Andy Shaughnessy
I-CONNECT007

I like to travel, even for work. I'm lucky that I don't have to do back-to-back turnarounds.

But after a week in Las Vegas covering IPC APEX EXPO and the Design Forum, I was happily flying back home on a half-full 757. When was the last time you had three seats to yourself? I counted back: 10 years ago, flying from Salt Lake City to Billings, Montana.

The Mandalay Bay Convention Center is a good venue for APEX, but you wind up walking 20 miles each day. Somehow, you're always one mile from where you need to be in 10 minutes.

The show kicked off with the Design Forum on Monday, March 23, with design experts speaking throughout the day. Editor Kelly Dack and I shot a variety of video interviews with the movers and shakers in the design community. It's always nice to catch up with PCB designers and design engineers. And I had to marvel at how Anne Marie Mulvihill, IPC's manager of design programs, managed to herd all these cats again for another year.

Speaking of IPC, I spoke with President John W. Mitchell and discovered that he lives near me in metro Atlanta, and he designed PCBs in the past. For years, PCB designers felt, often accurately, that IPC was giving the design community short shrift. But Mitchell sounded determined to change that. How many of you ever thought IPC would be led by a man who had PCB design experience?

During APEX, we held a panel discussion on data transfer formats, with Altium's Ben Jordan moderating. Karel Tavernier of Ucamco, which owns Gerber, joined Mentor Graphics' Dave Wiens, who represented ODB++, and Hemant Shah of Cadence Design Systems, who is active in developing the IPC-2581 standard.

Note: No one was injured during filming of this panel.

The data seem to favor ODB++ and IPC-2581, which were both developed precisely for transmitting PCB design data to manufacturers. Both are backed by technologists working to make these formats better. Both are clearly more efficient than Gerber, which was originally developed as a machine control language.

Yet most designs are still output in Gerber. We can publish article after article about the benefits of the newer formats, but designers still prefer Gerber. When I ask them why, they say that they're used to it, so what's the problem? Most designers have never used anything else. Will the designers of the future opt out of the tried-and-true Gerber?

Gold Watch Time?

So Rick Hartley is really retiring. From his "day job" at L-3, that is—not from PCB design instruction.

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OUT WITH THE OLD, IN WITH THE NEW? *continues*

Hartley broke this news during our interview at the Design Forum. He's been threatening to retire for years, but you know how it is with PCB designers.

PCB designers are always talking about retiring, or leaving the industry in general. Some designers say they want to chuck it all and become IT guys. But most of them are still designing boards.

And when they do eventually pack it in, what do designers do during retirement? They keep working in PCB design, but without worrying about the alarm clock five days a week.

Case in point: After years of talking about it, columnist and design instructor Doug Brooks finally retired from daily work at the service bureau he founded, UltraCAD Design. But he just wrote a book and published a series of instructional videos on signal integrity.

As Michael Corleone said in Godfather III, "Just when I thought I was out, they pull me back in."

Maybe designers really love their jobs after all. One thing is certain: Designers aren't complaining as much as they did. And I know, because they complain to me, as if I have the power to fix real and imagined slights in their workplace.

Of course, I can't get you a raise or increase your respect within the company. You are responsible for doing that. To paraphrase the soon-to-be-wearing-a-cardigan Hartley, it's up to you to be the go-to design expert, and a zealous advocate for PCB design within your company.

Are you that person?

Eventually, we're going to need a new cadre of PCB design instructors. If you're a veteran PCB designer (and you probably are) who is accustomed to public speaking, even just addressing your work group, you might be a good design instructor.

It's not a way to get rich. After a while, you'll make a few dollars, but you won't want to quit your day job. It might cover your travel and give you some money for video poker in Vegas. Some instructors say that when they figure in the spare time they devote to staying at the top of their game, they're making slightly over the minimum wage. It will take over a lot of your life, but if you love what you're doing, you won't mind.

Many design instructors publish a book or two, but that's mainly to keep their names in the public eye. In the long run, you're not going to make Stephen King cash writing about PCB design. That's partly because most designers want everything to be free. If you charge what your book is worth, some designers will take to the DC List complaining, "You want $79 for a book that explains everything I need to know about high-speed design? What a rip-off! Sure, it may make me a better designer, but if I buy that book, I'll go bankrupt! My kids will starve!"

> **"*In the long run, you're not going to make Stephen King cash writing about PCB design.*"**

No, most PCB design instructors are overworked and underpaid. But they are granted access to the closest thing to modern-day Camelot: the speakers lounge. Speakers who enter these hallowed halls are sworn to secrecy, but we've all heard rumors of the wonders within: exotic dancers, wet bars, two types of bagels, and wifi that never cuts off. Plus, you get to wear the ultra-cool speaker badge on your lanyard, and that's, well, priceless.

In the end, design instructors just have to love PCB design, and they have to love talking about PCB design. Does that describe you? If so, try teaching a class or two. The design instructors you know will be happy to help you dip a toe in the water.

It's easy to see that we're running out of PCB designers and design instructors. We need to do all we can to bring in new blood, or we're going to have a real problem one day. **PCBDESIGN**

Andy Shaughnessy is managing editor of *The PCB Design Magazine.* He has been covering PCB design for 13 years. He can be reached by clicking here.

video interview

Hartley on the Future of PCB Design Education

by Real Time with... The Design Forum

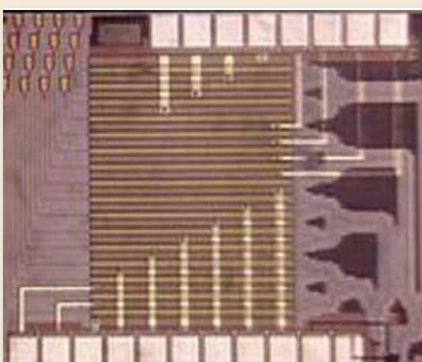
Now nearing retirement from his "day job," but not from PCB design, veteran instructor Rick Hartley waxes philosophical about the future of design and design education.

realtimewith.com

Bending Light with a Tiny Chip

Imagine that you are in a meeting with co-workers. You pull out your cell phone to show a presentation or a video on YouTube. But you don't use the tiny screen; your phone projects a bright, clear image onto a wall or a big screen. Such a technology may be on its way, thanks to a new light-bending silicon chip developed by researchers at Caltech.

The chip was developed by Ali Hajimiri, Thomas G. Myers Professor of Electrical Engineering, and researchers in his laboratory. The results were presented at the Optical Fiber Communication conference in San Francisco on March 10.



Traditional projectors pass a beam of light through a tiny image, using lenses to map each point of the small picture to corresponding, yet expanded, points on a large screen. The Caltech chip eliminates the need for bulky and expensive lenses and bulbs and instead uses an integrated optical phased array to project the image electronically with only a single laser diode as light source and no mechanically moving parts.

Hajimiri and his colleagues were able to bypass traditional optics by manipulating the coherence of light, a property that allows the researchers to "bend" the light waves on the surface of the chip without lenses or the use of any mechanical movement. If two waves are coherent in the direction of propagation, the waves combine, resulting in one wave, a beam with twice the amplitude and four times the energy as the initial wave, moving in the direction of the coherent waves.

MYTHBUSTING:

There are no One-Way Trips!

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

One of the greatest myths in PCB design is that we only have to route signal traces from pin-to-pin to make a complete connection. And, that ensuring these traces have matched delay is the only timing issue we need to consider. However, current is not a one way trip—it must complete the circuit back to the source in order to provide the round-trip current loop. This misconception comes from the fact that we only draw the pin-to-pin connections on the schematic and ground the chips at one point.

Current always flows in a loop. However, it does not go down to the end of the trace, to the load, and then begin to make its way back to the source. But rather, the outbound pulse charges the local parasitic capacitance as it propagates down the transmission line and returns to the driver. As the pulse progresses down the line, current returns to the source as the wave front moves until it finally reaches the load. If the return path is disrupted and does not flow directly beneath the trace, the loop area and hence delay are extended. This generally results in increased emissions of radiation.

In a previous column, The Dumping Ground, I discussed why the ground plane is not a dumping ground for unwanted signals. Most PCB designers think that the ground only serves to make the routing easier, allowing the designer to ground anything, anywhere without having to run multiple tracks. Generally, a component requiring a ground connect is just grounded at

any point on the board creating the connection. But this does not consider the return current path which is just as important as the actual trace routing for high-speed design.

In a DC circuit, the return current takes the path of least resistance. But at high speeds, the return current takes the path of least inductance which just happens to be the reference plane (either ground or power) directly above or below the trace.

The planes in a high-speed, digital board perform four crucial functions:

1. Provide a reference voltage for the exchange of digital signals
2. Distribute stable power to all logic devices
3. Control crosstalk between switching signals
4. Provide a shield for electromagnetic radiation on internal layers

Figure 1, illustrates the cross-section on a microstrip (outer layer) trace and its associated plane return current distribution (red). Where the electric fields (blue) are more tightly coupled to the plane—directly below the trace—the return current also exhibits tighter coupling. But where the field spreads out from the trace, the larger loop area, between the signal and the return current path, increases the inductance. Return current tends to couple to the signal conductor, falling off in intensity, with the square of increased distance. A stripline (inner layer) return current distribution is narrower with the fields more intense above and below the trace.

Because of the skin affect, the high-frequency fields cannot penetrate the plane and so the reference plane return currents will exist where the electric field lines terminate on the adjacent plane. Magnetic fields, which are not illustrated, circle the trace and radiate outward.

For a microstrip trace the return current density J(x) is given by:

Equation 1

$$J(x) = \frac{I}{w\pi}\left[tan^{-1}\left(\frac{2x-w}{2h}\right) - tan^{-1}\left(\frac{2x+w}{2h}\right)\right]$$

where:

- I is the total loop current
- x is the horizontal distance out from the centre of the trace
- w is the width of the trace and
- h is the distance of the trace from the plane

The current density will be the same regardless of the frequency. The only constraint is that the frequency is high enough so that the resistance of the plane is negligible, compared with the inductive reactance. Typically, this occurs at frequencies above a few hundred kilohertz, which means basically any digital PCB.

Crosstalk between adjacent traces (edge-coupled) is the result of the interaction of these fields.

Equation 2

$$Crosstalk = \frac{h^2}{x^2}$$

Equation 2 shows that the crosstalk between adjacent microstrip traces is proportional to the

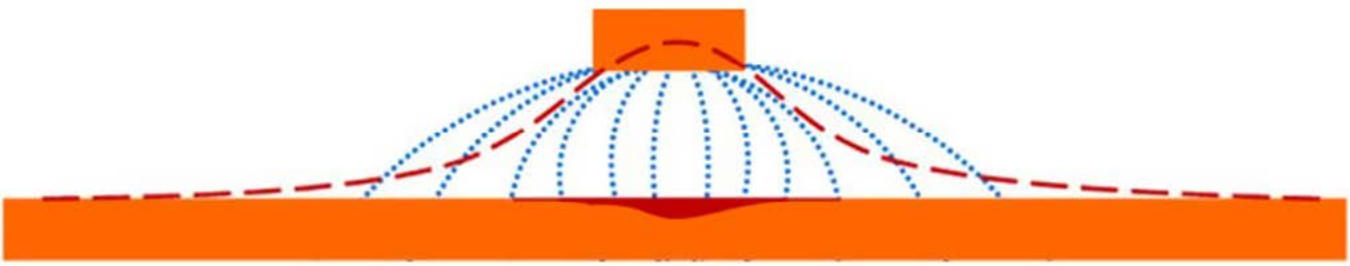
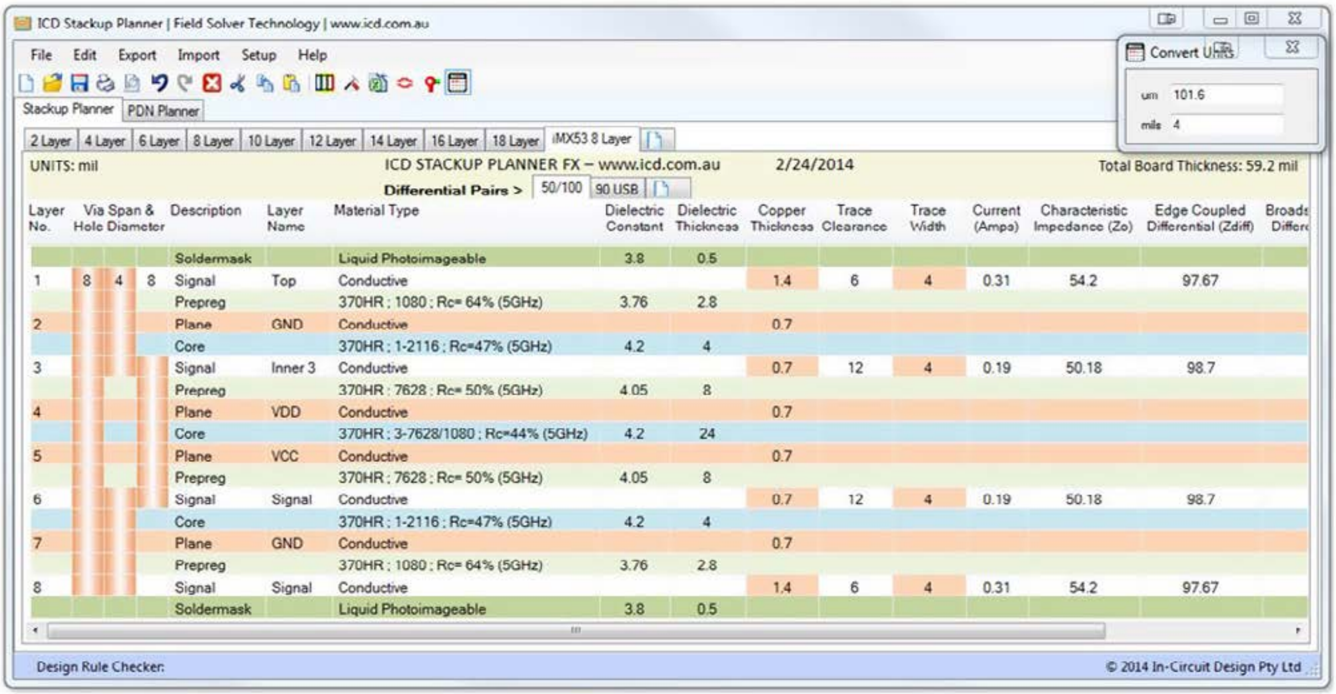


Figure 1: Microstrip plane return current distribution.

MYTHBUSTING: THERE ARE NO ONE-WAY TRIPS! *continues*



Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Liquid Photoimageable	3.8	0.5						
1	8 4 8	Signal	Top	Conductive			1.4	6	4	0.31	54.2	97.67
		Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8						
2		Plane	GND	Conductive			0.7					
		Core		370HR ; 1-2116 ; Rc=47% (5GHz)	4.2	4						
3		Signal	Inner 3	Conductive			0.7	12	4	0.19	50.18	98.7
		Prepreg		370HR ; 7628 ; Rc= 50% (5GHz)	4.05	8						
4		Plane	VDD	Conductive			0.7					
		Core		370HR ; 3-7628/1080 ; Rc=44% (5GHz)	4.2	24						
5		Plane	VCC	Conductive			0.7					
		Prepreg		370HR ; 7628 ; Rc= 50% (5GHz)	4.05	8						
6		Signal	Signal	Conductive			0.7	12	4	0.19	50.18	98.7
		Core		370HR ; 1-2116 ; Rc=47% (5GHz)	4.2	4						
7		Plane	GND	Conductive			0.7					
		Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8						
8		Signal	Signal	Conductive			1.4	6	4	0.31	54.2	97.67
		Soldermask		Liquid Photoimageable	3.8	0.5						

Figure 2: An 8-layer stackup using Isola 370HR, 5GHz material.

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Liquid Photoimageable	3.8	0.5						
1	8 4 8	Signal	Top	Conductive			1.4	20	12	0.69	50.19	98.28
		Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8						
2		Signal	Inner 2	Conductive			0.7	15	4	0.19	50.7	98.52
		Prepreg		370HR ; 1080 ; Rc= 64% (5GHz)	3.76	2.8						
3		Plane	GND	Conductive			0.7					

Figure 3: 10-layer buildup alternative stackup (only top shown).

square of the trace height above the plane divided by the square of the separation distance. This illustrates an important point: that placing the trace closer to the reference plane will reduce crosstalk even if the trace spacing remains the same. This provides an effective way to reduce crosstalk without using up valuable real estate on the board which would be the case if the trace separation were increased.

Now that we have established the fact that the return current follows the path of least inductance, and that it has a defined distribution in the reference plane, we need to now look at how the return current propagates in the planes.

Figure 2 shows the ICD Stackup Planner[4] creating an 8-layer stackup for an iMX53 processor and DDR2 memory combination. In this case, layers 1 & 3 and layers 6 & 8 are used for the layer pairs and all routing encircles the ground planes on layers 2 & 7. Since the ground is referenced in all cases, ground stitching vias can be placed near layer transitions (vias) to allow the return current to change planes where required. This limits the loop area, and hence the radiation.

Or, would a buildup microstrip layer be better if you are risk-aversive? In Figure 3, I have added another buildup layer to the stackup (top and bottom). Copper plating on outer layers attributes considerable variations in trace width and thickness, hence impedance variations. You should avoid routing controlled impedance signals on these layers, but they can be used for

pads/lands and traces that are non-critical. Via-in-pad could be used or a just short (<200mil) fanout to layer 2 using a 12 mil trace in an attempt to maintain impedance.

In order to change reference planes:

- If there are multiple ground planes, then place a stitching via as close as possible to each layer transition (signal via)
- If power planes are also used as the reference plane, then place decoupling capacitors as close as possible to each layer transition

When you plan your stackup, be aware of which planes—either power or ground—will be the return path for your critical signals and make sure there is an unobstructed return path. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane: Where is the best place for the current to flow, and is it unobstructed? The reference plane(s) adjacent to each signal layer allows the return current to flow as closely as possible to the signal trace, reducing inductance and loop area. A large loop area will create higher emissions of electromagnetic radiation, so we need to keep these as tightly coupled to the trace as possible.

The best way to go about this is to look at each signal layer with respect to its associated reference plane. Figure 3 shows an internal signal layer and the ground plane. Make sure that there are no large cut-out areas or lines of anti-pads on connectors that completely block off the ground, forcing the return paths to deviate from their associated traces. This is best done in a CAM/Gerber viewer as what you see—is what you get. Whereas, in the CAD database you may not see the correct anti-pad or plane cut-out sizes. You may have to reduce the size of the anti-pads if they are too close. SMT boards are not so bad, in this respect, but through-hole connectors generally create issues.

Also, keep in mind that high speed signals

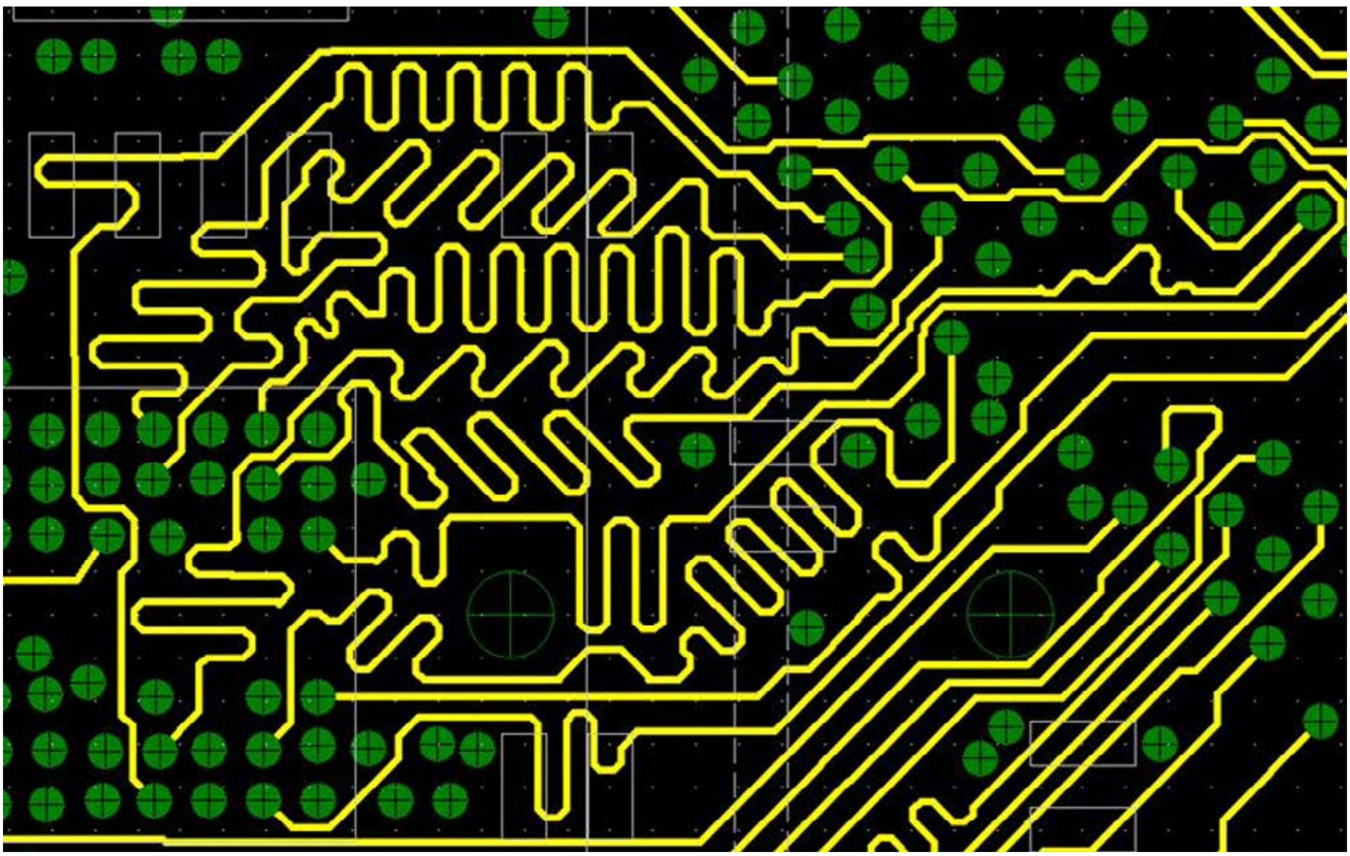


Figure 4: Signal layer 3 with respect to ground plane layer 2.

should not be routed on the outer layers. Embedding the signals between the planes (on layers 3 and 6) reduces the radiation by at least 10 dB. So fanout from the driver and drop to the internal signal layer routing up to the load through a short stub.

In conclusion, apart from routing pin-to-pin, it is important to also consider how the return current propagates in the planes. When you plan your stackup, be aware of which planes—either power or ground—will be the return path for your critical signals and make sure there is an unobstructed return path.

Points to Remember

• Current always flows in a loop. The outbound pulse charges the local parasitic capacitance as it propagates down the transmission line and returns to the driver.

• The ground plane is not a dumping ground for unwanted signals.

• In a DC circuit, the return current takes the path of least resistance.

• At high speeds, the return current takes the path of least inductance which just happens to be the reference plane (either ground or power) directly above or below the trace.

• Return current tends to couple to the signal conductor, falling off in intensity, with the square of increased distance.

• Because of skin affect, the high-frequency fields cannot penetrate the plane.

• The current density will be the same regardless of the frequency.

• Placing the trace closer to the reference plane will reduce crosstalk even if the trace spacing remains the same.

• It is important to consider how the return current propagates in the planes. When you plan your stackup, be aware of which planes—either power or ground—will be the return path for your critical signals and make sure there is an unobstructed return path.

• If there are multiple ground planes, then place a stitching via as close as possible to each layer transition (signal via).

• If power planes are also used as the reference plane, then place decoupling capacitors as close as possible to each layer transition. **PCBDESIGN**

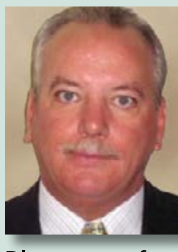
References

1. Barry Olney Beyond Design columns – The Dumping Ground, Embedded Signal Routing

2. Howard Johnson—High-Speed Signal Propagation

3. Henry Ott—Electromagnetic Compatibility Engineering

4. The ICD Stackup Planner and PDN Planner can be downloaded from www.icd.com.au



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

Single-Atom Light Switch

With just a single atom, light can be switched between two fibre optic cables at the Vienna University of Technology.

Scientists are trying to build optical switches at the smallest possible scale in order to manipulate light. At the Vienna University of Technology, this can now be done using a single atom.

Researchers capture light in so-called "bottle resonators." If such a resonator is brought into the vicinity of a glass fibre which is carrying light, the two systems couple and light can cross over from the glass fibre into the bottle resonator.

The atom can be prepared in such a way that it occupies both switch states at once.

Mythbusting: Semi-Additive Process Makes Sub-3/3 a Reality

by Amit Bahl
SIERRA CIRCUITS

Prudent PCB designers used to have good reasons for avoiding trace widths and spaces smaller than 3 mils beyond very short spans. But the 3 mil limitation is now becoming a thing of the past, thanks to the use of semi-additive fabrication by some board manufacturers. The main reason designers steered clear of sub-3-mil lines and spaces for more than short distances is etch factor.

The convergence of ever-greater circuit density and ever-higher data rates has reached the point where the chemistry of conventional PCB fabrication processes cannot be controlled tightly enough to consistently satisfy design needs. The traditional manufacture of PCBs begins with a laminate clad with copper on one or both sides. PCB manufacturers purchase clad laminates (cores) from suppliers in a wide range of substrate materials and copper thicknesses, and they also create laminates by bonding substrate materials in prepreg form with copper foils in a press.

Basically, traces are patterned by applying an etch resist to the copper surface, curing the resist by selectively exposing it to light where copper should be retained as traces and other features, and then etching away (subtracting) the unexposed resist and underlying copper in an acid bath. The objective is to produce traces whose cross-section is rectangular. However, the bath not only removes copper in the vertical direction but also eats some of it away at the sides of the traces horizontally underneath the resist, resulting in the sort of profile illustrated in Figure 1 [1].

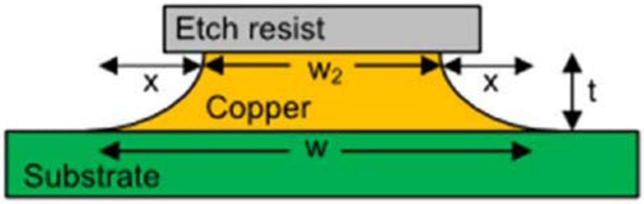
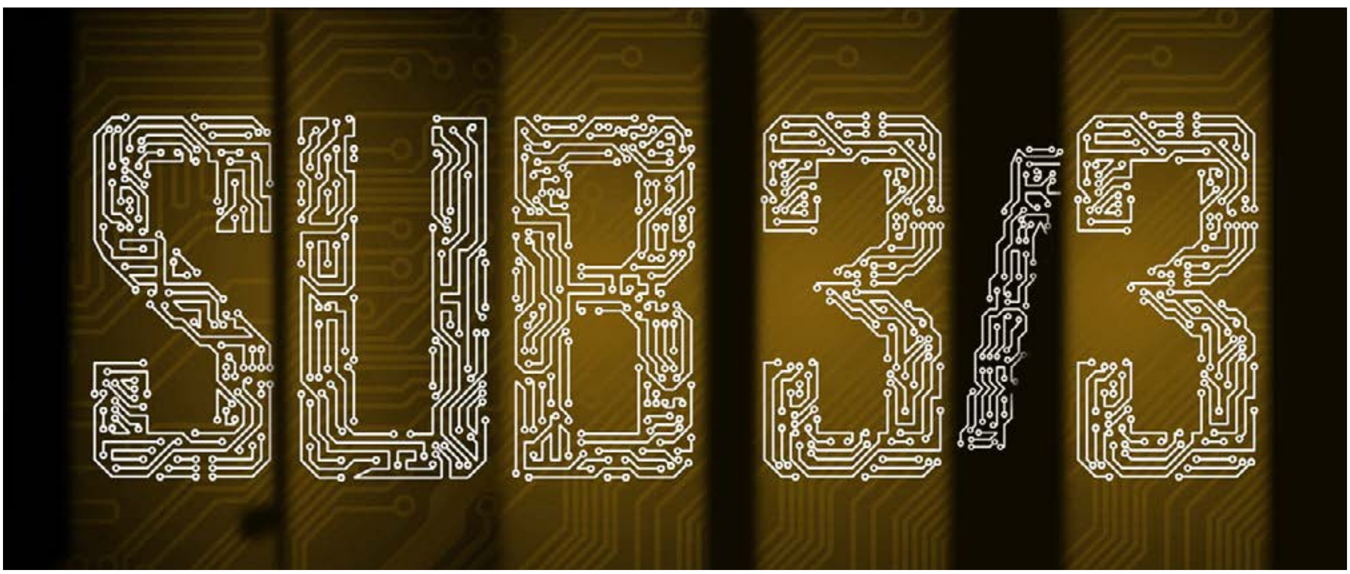


Figure 1: The etch factor (F) is the ratio of the trace height divided by how far the trace was eaten away at the top on one edge compared to the base. F = t/x.



A well-controlled subtractive process repeatedly produces traces that are approximately trapezoid in cross-section, whose sides are at a 25–45 degree included angle from the base, while the base is at design width. But bath chemistry can vary and traces can be over-etched, further diminishing their cross-section such that their top surface is much narrower than the base. The ratio between the height of the trace post-etch (t) and how far the trace has been eaten away at the top of an edge (x) is the etch factor (F). The higher the etch factor, the better the trace section resembles an ideal rectangle, provided the base is at design width. Bath chemistry can also vary such that too little copper is removed and traces at their base extend beyond design width.

At best with the subtractive process, the width of a trace at the top and at the base can be held to within 0.5 mil of design value. Such a tolerance has little consequence when traces and spaces are 3 mils or wider and signal edge rates are low. However, it has a significant effect on the characteristic impedance of thinner traces and a profound influence if those narrow traces are tightly coupled differential pairs in high-speed digital circuits. Moreover, the smaller the area of a trace cross-section is compared to an ideal rectangle, the worse the IR loss becomes along the trace. The closer a trace cross-section matches an ideal rectangle, the closer it comes to matching the characteristic impedance desired by the PCB designer.

If traces could be fabricated at design width with nearly vertical sides, the maximum circuit density could be achieved, signal integrity could be ensured, and PCB yields could be optimized. That is the case with the semi-additive fabrication process.

In contrast to the trace geometries that result from the subtractive process, which are chemistry- and process-defined, the trace geometries from the semi-additive process are lithographically defined. Photolithography creates a well-defined trace. Trace width and spaces produced by the semi-additive process are extremely close or identical to the as-designed dimensions.

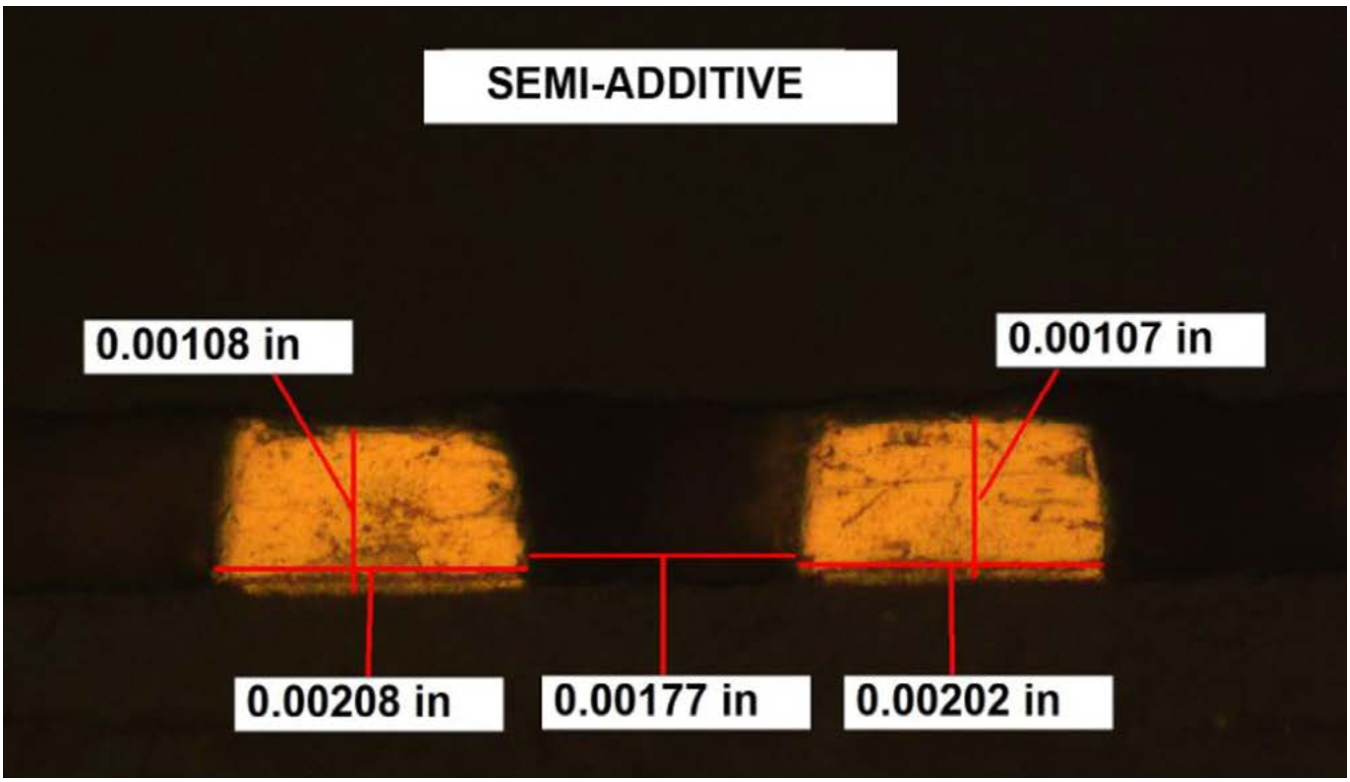


Figure 2: A typical cross-section along a pair of 2 mil wide traces on 1.8 mil spacing formed by the semi-additive process. Note the near-vertical sides.

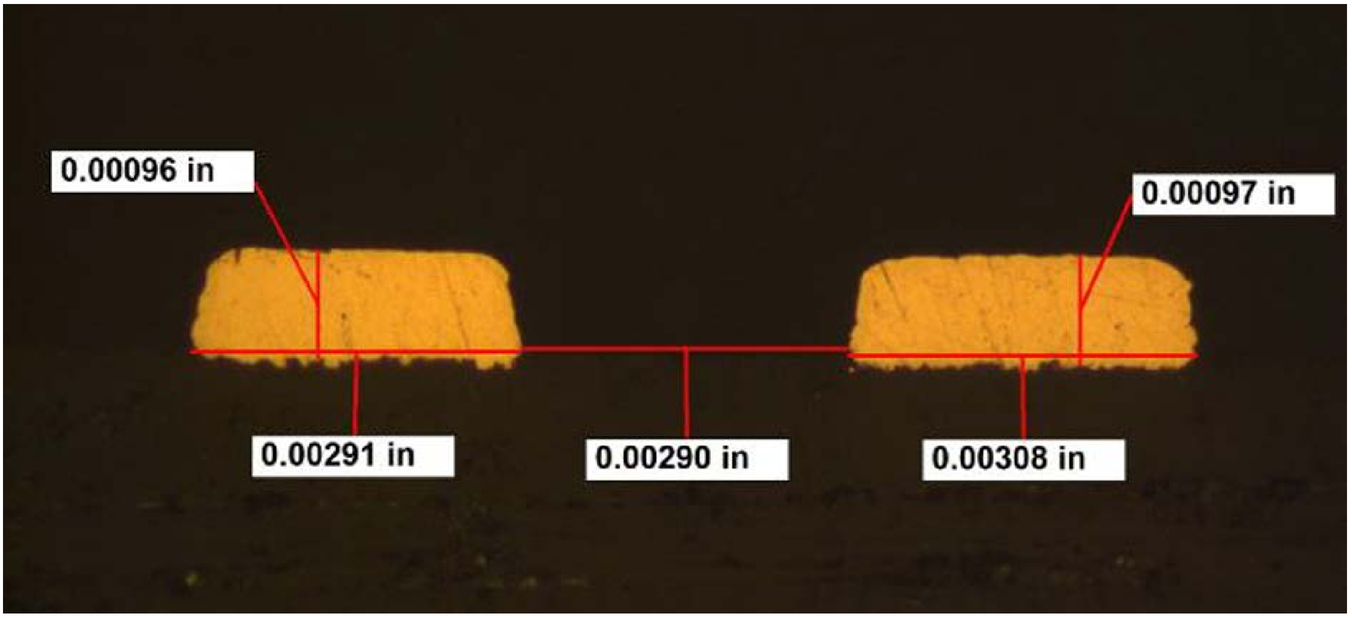


Figure 3: This pair of traces designed to be 3 mils wide on 3 mil spacing was produced by the best possible subtractive process.

The semi-additive process is essentially the opposite of the subtractive PCB fabrication process. It starts with a laminate that is clad with much thinner copper than the thinnest conventional foils. For example, quarter-ounce copper is approximately 8.5 µm thick, but the ultra-thin foil is typically 2 µm or 3 µm thick. Such ultra-thin foils have a backing that is removed after the foil is laminated to the substrate. The holes are drilled and then a bath of electroless copper coats the bores and the foil surface. A "reverse" resist is applied, developed, and selectively removed to expose only the areas that will become the traces, vias, and other conductive features. Those exposed areas are plated up, the resist is stripped, and the ultra-thin copper remaining in the well between the conductors is etched away.

The plated-up traces and features are far more accurately defined than those produced by even the most-well-controlled subtractive processes (Figures 2 and 3). Trace width and spacing down to 1.25 mils can be maintained over distance within extremely tight tolerance. There is no penalty in manufacturing time. The semi-additive process frees designers who would otherwise be challenged to break-out dense fine-pitch BGAs and also enables very strict impedance control to ensure signal integrity.

And finally, while I have the chance to dispel myths harbored by some PCB designers, let me clear up another misconception. If any manufacturer tells you there's a setup charge for board fabrication or assembly, tell them no thanks, you'll shop elsewhere.

Remember, no special jigs or one-off fixtures are necessary to build these boards. Tell them I said so. **PCBDESIGN**

References

1. Abdelghani Renbi, Arash Risseh, Rikard Qvarnström, and Jerker Delsing, "Impact of etch factor on characteristic impedance, crosstalk and board density," IMAPS 2012.

Amit Bahl directs sales and marketing at Sierra Circuits, a PCB manufacturer in Sunnyvale, California. He can be reached by clicking here.

PCB007 News Highlights

MFLEX Announces Restructuring Plan

Following a full review of its manufacturing footprint and in an effort to realign its manufacturing capacity and costs with expected revenues, MFLEX is consolidating its production facilities to reduce the total manufacturing floor space by approximately one-third.

IPC: N.A. PCB B2B Ratio Improves, Sales Lag

"January is typically a slow month in electronics manufacturing, especially compared to December, but this winter the industry may also be feeling the effects of weather-related slowdowns," said Sharon Starr, IPC's director of market research.

IPC: Flexible Metal-clad Dielectric Materials Standard

This standard establishes the classification system, the qualification and quality performance requirements for flexible metal-clad dielectric materials to be used for the fabrication of flexible printed circuitry and flexible flat cable.

Flexible PCB Market Expected to Reach $12B in 2014

The global flexible printed circuit board (FPCB) market valued US $11.3 billion with a YoY growth rate of 9.4% in 2013, and will be worth $12 billion in 2014 and US $12.68 billion in 2015.

Sunstone Circuits Announces On-Time Guarantee

The Sunstone On-Time Guarantee is a first in the PCB industry, and does not include numerous restrictions and rules that would void its usability. The guarantee will provide more value and peace of mind for design engineers as they quote and order their boards.

Newbury Electronics Installs UK's First UV-P300 LDI

The new machine, a UV-P300 LDI, is manufactured by Limata, and uses the latest in laser technology to produce far more technically demanding PCBs than could be achieved using the more traditional photo lithographic techniques.

Ray Young Appointed GM of Ventec USA's CA Division

Ray Young brings with him over 40 years of experience in PCB manufacturing at all levels from hands-on processing through plant management and general management to senior operations executive roles in industry-leading companies supplying the high-technology, high-reliability electronics industry.

i3 Electronics Achieves Critical Re-certifications

i3 Electronics has recently completed assessment for re-certification to several critical Quality Management Standards including AS9100C (Aerospace, Military, and Defense Standard), ISO 9001:2008 (General Quality Systems), and ISO 13485:2003 (Medical Devices). All three certifications were achieved with zero nonconformances.

Cicor's PCB Division Reports Positive 2013 Results

In 2013, Cicor Group experienced a healthy growth in revenue and was ab le to further increase its competitiveness. All divisions performed well in the medical field, an area Cicor has particularly focused on for some time now. The medical segment has become the Cicor Group's biggest market segment with 28%. Revenue growth rates varied among the divisions.

WEdirekt Online PCB Shop Achieves Over 40% Growth

With strong revenue growth WEdirekt, the online circuit boards store at Würth Elektronik has managed an extremely successful year in 2013. The order intake at WEdirekt increased by approximately 40% this fiscal year. Carina Harnisch, the head of WEdirekt, has developed ideas and targets for 2014 to increase this success even further.

EDA Mythbusters: Time for a New Era

by Abby Monaco, CID
INTERCEPT TECHNOLOGY

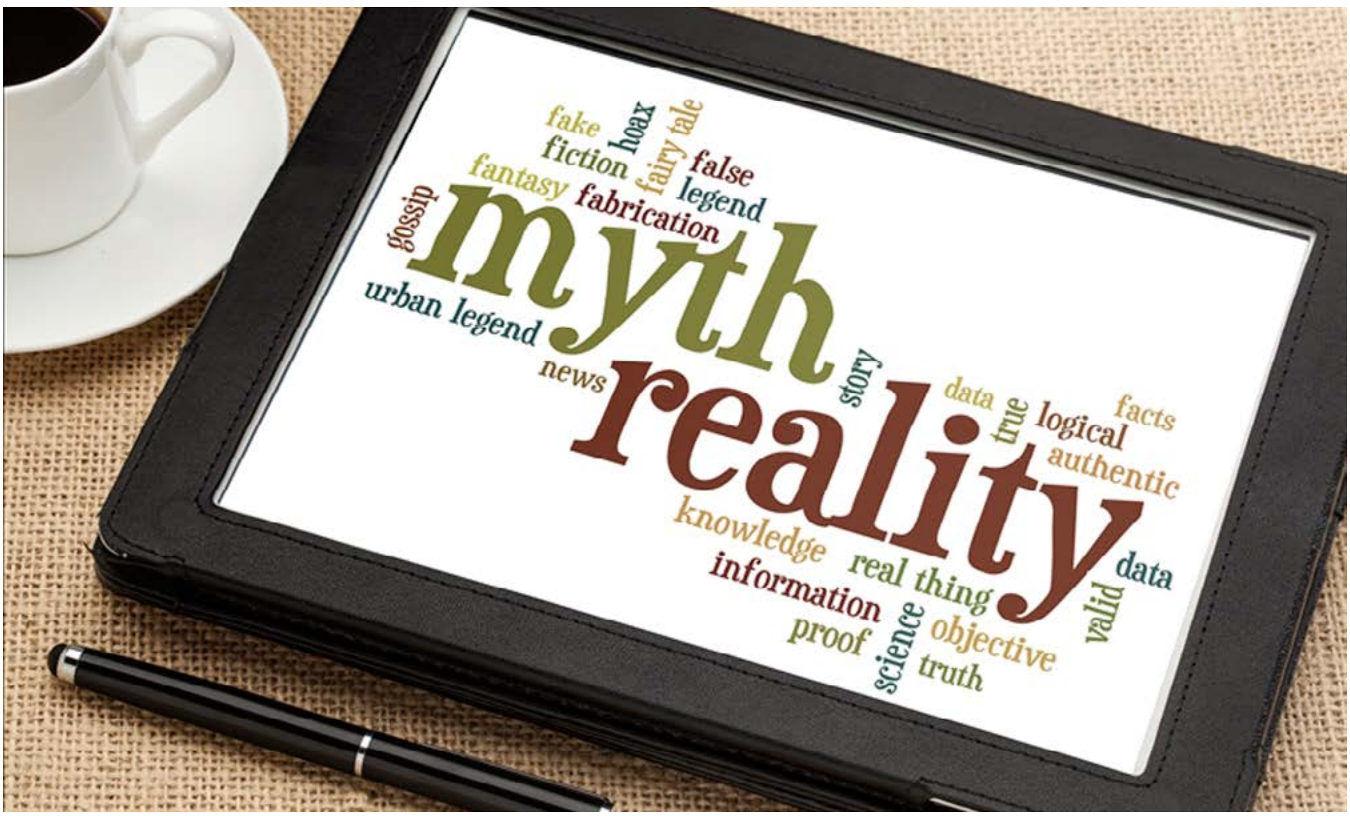
Like many communities, the EDA industry has its share of myths. But rather than quoting statistics and studying the issue, I thought I could share how my own experiences in EDA have debunked these myths. I imagine that many of your experiences probably have busted these myths as well.

With the constant shifts in the tech world, it's time to draw a line and start a new era. And it's not a man's world anymore: just look at all the female executives in high-tech, like Yahoo CEO Marissa Mayer. It's time to stop looking back, stop maintaining the status quo, and start innovating again. Throw the old standards out the window! Let's lift our thoughts out of the bits and bytes and into the quantum. Let's get started!

Myth 1: Engineers are Dorks

Well, maybe they are. But I have news for you: Dorks are cool. Just look at the massive popularity of "MythBusters" and "The Big Bang Theory." Then look around you. We work in an industry that is full of the coolest dorks ever!

At work, I sit next to a banjo player who has an elaborate setup in his basement for drying habanero peppers. (No, it's not a cover for weed. He really dries peppers, and only peppers.) Across the hall is a father of three who home-schools his kids, learned to play the guitar in his 30s, and enjoys whiskey sours with his wife on spring weekends. Next to him is our Israeli mastermind, who once worked for Ucamco, sold two of his own startups, and only speaks to offer hilarious quips or point out our shallowness.



Also among our ranks is a deep-sea fisherman, a hiking aficionado, a vegetable farmer, an expert pub crawler, and much more I've left unmentioned. These guys are so interesting, entertaining, smart, and darned productive at work. I admire every one of them.

Let's all be dorks together! I love this industry.

Myth 2: PCB Designers are Just CAD Monkeys

This one can really get my blood boiling! I can feel the heat of yours too. My first years in EDA were spent training to be a PCB designer. When I rubbed up against the EEs in my company, they would scoff at me like I was some bottom-feeder trying to get into the "in" crowd. I couldn't understand this, because I was pulling in big contracts for my company. What did it matter if I went to a five-year university as opposed to learning a trade on the job?

But you all know you are not CAD monkeys! The training, experience, and creative aspects that go into designing a board have gotten more complex over time. And while many of the EEs are tied more closely to the physical design of the board now, a whole lot of them still need the experienced designers to complete a successful layout. Things may change over time, but I have no end of respect for the older designers who had to lay out boards with primitive systems, and the newer designers who have to understand sophisticated software to accomplish a difficult task. Keep up the great work, folks!

Myth 3: Girls Can't Work in Engineering

As an athletic youth, I decided that I would prefer to be a boy. Boys could run faster, bike farther, and climb higher. I was so frustrated that I couldn't do the same, until my mother asked me, "Why not?" So I set out to be the quintessential tomboy, running the boys off the streets with my dirt bike, killing them in basketball, and generally emasculating them at every turn. I was bewildered as a senior in high school when I lamented to a past flame that it seemed like no boy ever "liked" me. He said, "Abby, you're one of the guys."

After college, I was recruited into Intercept Technology as a database translation expert; this had been my summer job throughout high school and college. Migrating customers to our software was a full-time job back then, with all the shifting the EDA industry was doing, not to mention the incredibly slow processors on our motherboards.

When I was moved to the Mozaix project, our electrical engineering schematic application, the waves of effrontery were palpable. The notion that a non-engineer, and a girl at that, could have any input on whether a schematic application worked properly caused my manager to go into fits of rage on a daily basis. I was told that I was too stupid to run this high-level software (yes, I really was told that), and that it didn't work for me because I had no idea how engineers do things.

"The notion that a non-engineer, and a girl at that, could have any input on whether a schematic application worked properly caused my manager to go into fits of rage on a daily basis. I was told that I was too stupid to run this high-level software (yes, I really was told that), and that it didn't work for me because I had no idea how engineers do things."

Someone at the top could see something I couldn't. My manager was eventually fired, and I was promoted deeper into the project. I'm now the product manager for that project and others, and most of what I designed and implemented since then was accomplished with the help of very intelligent engineers. These engineers work side by side with me every day. Granted, it took many years to earn their respect, but persistence was the key. For all women in this field, I can only say that confidence and persistence is everything. For some of the less open-minded men, I would like to ask that you try a little more respect up front so we can all get more work done without the tension. The female brain can do a lot of amazing stuff, so eyes up, boys.

Myth 4: "I just want it to work."

Uh-huh. Sure you do.

One segment of my life working on the Mozaix project was the "Get it to Work" phase. This was Mozaix 1.0. It was awful! I spent about three years just getting the thing to work. By Mozaix 2.2, it was stable and customers were coming aboard. But I cannot tell you how many phone calls I took from people telling me that the way the program worked was stupid, ugly, frustrating, and plenty of other expletives that you can imagine.

No, EDA engineers don't just want their software to work. They want it to be easy. They want it to be pretty. They want it to make your coffee for you and rub your shoulders while it produces your design quickly. Engineers tend to have that functional way of looking at things—if it works, the world is happy. But it's not that simple. It's HOW it works that is everything. This rule permeates far beyond software, but for many engineers, the notion still eludes them.

So, after my years of being verbally pummeled on the support lines, I was moved into a product manager position and tasked with making the program work nicely. It was a lot of fun to come full circle; I started with a manager who wanted to spit on my requests to "Make it pretty," as he would leeringly say to me. I ended up being the one in charge of doing just that.

So with Mozaix 3.0, I had the pleasure of working with a great team of young engineers, and we proceeded to revamp, redesign, upgrade, and "pretty up" a program that worked, in addition to working the way you wanted it to word. Since that time, support traffic has dropped to an all-time low. So don't tell me you just want it to work—next time, tell me how you want it to work. It takes collaboration, fresh ideas, and just a little extra involvement from a user to really hit the solution out of the park. I'm listening.

> ***"No, EDA engineers don't just want their software to work. They want it to be easy. They want it to be pretty. They want it to make your coffee for you and rub your shoulders while it produces your design quickly. Engineers tend to have that functional way of looking at things—if it works, the world is happy. But it's not that simple."***

Myth 5: Atlanta is Full of Rednecks

Since much of our industry is concentrated on the West Coast, I'd like to set this one straight. The largest city in the South is not full of rednecks. I am one of the few Atlantans who actually grew up here; most Atlantans are transplants who moved here from other parts of the country, usually to take advantage of the warmer weather. I do not have a "Suthun" accent. No one I know chews tobacco. One thing you may find interesting is that Atlanta has more oversized SUVs than humans. What's even more interesting is that half of these SUVs are blinged up, and the other half are driven by moms. I'm more scared of the moms. The blingy guys are fine by me. Quite a few live in my neighborhood, and these folks come in all colors and creeds. In Atlanta, I think every color and creed is a minority. There is no majority of anything—it's one big melting pot. Atlanta is the essence of America.

Myth 6: PCB Design Tools are All the Same

I've seen comments like this on LinkedIn discussions over the years. I've also seen die-hard followers who would never consider using a different tool from their favorite. Everyone has a different opinion, but one thread that seems to hum regularly is people asking what makes some software packages better than others. It is true that they can all do the job of laying out a schematic and designing a board. But we all know that the term "board" is an overly broad statement.

In order to assess the PCB tool that is right for you, you have to review your entire design process, decide if there are parts of it that need to change, look at the size and complexity of what you're doing, review all of the software packages available to you, and then repeat. Far too often, high-level management thinks it can slash the software budget because there are cheaper tools available. So they slash that budget, and project cycles suddenly double or triple, because the cheap software can't handle the complexity of the design at hand. Or worse, management enjoys getting fancy dinners and vacations from the high-end tools, so they continue to pay far more money than necessary for a software package that may or may not actually satisfy users' needs.

If you talk to a vendor, of course they'll tell you that his tool is the best thing for you. Quite honestly, what I know about all of the EDA PCB design tools could make me a free agent for every EDA software vendor out there. Sure, I'd love to see Intercept selling more Pantheon and Mozaix, but the truth is that it's just not going to be a perfect fit for everyone. We have great RF capabilities, some really cool auto-interactive routing options, the best design reuse blocks out there, and some great high-speed tuning functions. But do you need these things?

You need to decide for yourselves, and work hard to keep the upper management in tune with you. Blind, line-item budget slashes are the stupidest moves a manager can make. Don't let them do that to you! Get the tool that is right for the job, whether it be cheap or expensive. It directly feeds the productivity of the company, and someone at a higher level in a company should darn well recognize that! Time is money, so don't waste time on the wrong software package.

These are just some of the myths I've come across. Let's move past this sort of thing, and take EDA tools into a new era. **PCBDESIGN**

Abby Monaco, CID, is a director of products and marketing for Intercept Techology. She can be reached by [clicking here](#).

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video interview

Greg Munie Discusses DFX and Quest for New Blood

by Real Time with... The Design Forum

IPC's Greg Munie explains the association's focus on DFX, and the ongoing search for new, younger members who will carry the torch as baby boomers start to retire.

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IPC APEX EXPO 2014: The Opening Keynote Session

by Peter Starkey
I-CONNECT007 TECHNICAL EDITOR

Images contributed by Michael Weinhold

We will rock you! A grand Las Vegas opening to the 2014 IPC APEX EXPO included a spectacular show by dance troupe Speed of Life, complete with silver paint, angel wings, rollerblades and stilts. The approximately five-minute performance heralded the appearance of IPC President John Mitchell, who welcomed a packed house in the Mandalay Bay Convention Center, and declared the event's theme: New Ideas for New Horizons.

John Mitchell

Steve Pudles

Mitchell began by taking a few minutes to commend the success of the new IPC Validation Services initiative, and to present a certificate to IEC Electronics as the first company to be admitted to the Qualified Manufacturers Listing. After acknowledging the winners of the Best Technical Papers awards, Mitchell handed off to IPC Chairman Steve Pudles, who took the stage to introduce the keynote presenter, Dr. Peter Diamandis, co-founder and chairman of the X-Prize Foundation and co-founder of Singularity University.

Dr. Diamandis' provocative and inspirational presentation, "Creating a World of Abundance: Exponential Technologies Causing Disruptive Innovations," contained some sometimes frightening observations on the potential for future technology and other emerging market forces to dramatically influence living standards. Compared with human society's historical "local and linear" process of communication and development, where progress happened one step at a time, and the transfer of knowledge was limited by the distance a man could walk in a day, we are now in a world where progress is happening exponentially, and knowledge can be transferred anywhere in the world in a split second. He demonstrated how, in a company, these changes were accelerating disruptive stress—or disruptive opportunity depending on management's attitude to innovation. Agility is critically important. Companies commonly have experts who effectively block innovation by finding lots of ways an objective could not be achieved, and Dr. Diamandis despaired of organisations that start off with a mission and then back off because they decide it is too risky.

Nominating Kodak as the definitive example of a company worth billions that failed to recognise the disruptive opportunity presented by the digital camera in 1996—actually invented by one of its own people—and found itself overtaken by new technology and bankrupt in 2012, Dr. Diamandis noted that in contrast, in 2012, Facebook made a multi-billion-dollar takeover of Instagram, a young company of 13 employees. The life-span of a typical company is now of the order of 15 years, and he predicted that 40% of existing Fortune 500 companies would be out of business within the next 10 years.

Returning to the theme of local-and-linear thinking, Dr. Diamandis explained the philosophy of Singularity University in the study of exponential technology—with the example that thirty linear steps would gain a distance of thirty metres, whereas thirty exponential steps would circle the world twenty-six times. And Moore's Law exemplified the exponential growth in computing power, to almost inestimable levels in the future.

Near-infinite computing power could open up new dimensions in artificial intelligence—the ability to look beyond plain logic, even recognise the subtleties of irony, cynicism and humour, and understand what answer is relevant. Couple this with robotics, where a paradigm change is well underway, and truly intelligent machines are already a reality, as demonstrated in Dr. Diamandis' video of the view from the passenger seat as Google's autonomous car negotiated a slalom course at high speed. 3D printing is another area of exponential development, with amazing engineering capabilities. Breakthroughs in genome sequencing have enabled developments in synthetic biology to the extent that printed DNA molecules have been produced.

It was clear that the rate of innovation is exploding, and innovation is coming from everywhere. True breakthroughs generally come from unexpected directions. Dr. Diamandis made it plain that any company relying only on innovation from within was probably going nowhere and that to limit risk was to accept a future of, at best, incremental improvement.

Diamandis is a great believer in crowdsourcing. Lindberg flew the Atlantic to claim a $25,000 prize. Diamandis had a longstanding ambition to get into space. How? By throwing out the challenge to the world and offering a $10 million X-Prize as the incentive, which resulted in 26 teams spending a total of $100 million. "Set a target and challenge the world to solve the problem. Winner takes all—no second prizes!" He believes the world's biggest problems present the world's biggest business opportunities.

A question from the floor related to schoolchildren having little interest in taking up careers in science and engineering: How to inspire them? Dr. Diamandis suggested the answer was to make the scientists and engineers the rock stars, and to encourage the young people to perceive them as role models. The question he posed was, "How about a competition for the youngest person ever to travel to the space station?"

What is the next X-Prize challenge? Healthcare—to develop a hand-held universal medical diagnostic device. And after that, to achieve global literacy, even in the most impoverished areas.

Dr. Peter Diamandis

Dr. Diamandis' closed by declaring, "The only constant is change, and the rate of change is increasing. The next twenty years are going to be transformational. There's lots of change ahead, and the rate of change is increasing beyond our ability to project it!"

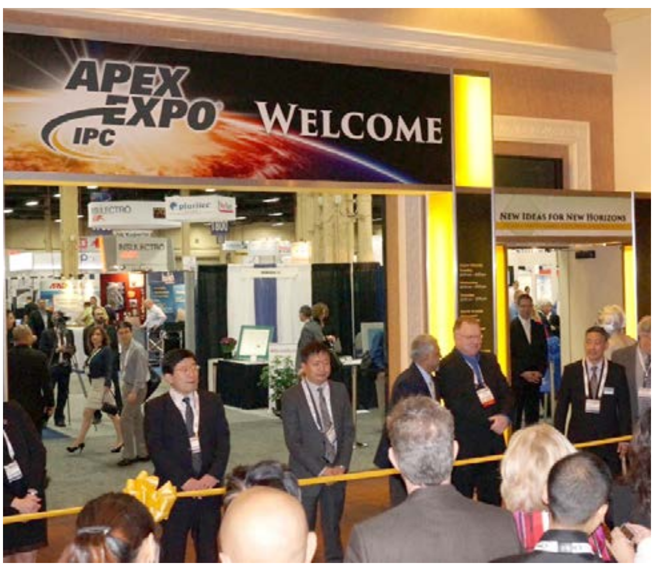
IPC APEX EXPO 2014: Publisher's Report

by Ray Rasmussen
I-CONNECT007

A sold-out show, record conference attendance and solid floor visitors made for a good show and conference at this year's IPC APEX EXPO in Las Vegas.

Here are some of my highlights.

Mentor introduced a major new software suite designed to remove the information barriers created by disparate systems. The software streamlines the design-to-fab-to-assembly information flow. Not being a user of software for design, fab or assembly, I can't speak to the software's effectiveness but, conceptually, it's a great idea and one that's been talked about for years. In fact, IPC hosted a meeting over a decade ago, which was well attended, and dealt with the communications issues in the supply chain. Think of how far along we'd be if that effort had gained traction. It's definitely a move in the right direction.



The *Printed Circuit Handbook, 7th Edition* is in the works. Editor Clyde Coombs came out of retirement to tackle the latest update of the PCB industry bible. First published in 1967, Coombs says this edition will likely contain up to 20% new content with all chapters getting significant updates, as needed, from some of the industry's leading experts. It's a labor of love for Coombs, who spent much of his career at HP in their PCB facilities. He says the book effort helps him stay connected with the industry.

Printed electronics, in its first-ever all-day session at an IPC event, offered a series of presentations from materials suppliers as well as PE makers, demonstrating the interest this technology is generating. In addition to the conference, an entire day was dedicated to standards development efforts. Marc Carter stated that IPC is working with organizations around the globe to develop the standards needed for this rapidly evolving industry. Currently, all of the standards IPC is working on are co-authored with JPCA. At this point in time, IPC is a leader in the development of PE standards for PE materials.

Walt Custer gave quite an upbeat assessment in his state-of-the-market report. All indications point to a year of good industry growth for most regions. The U.S. should see solid growth while Europe may see some growth, but will likely remain flat. Of course, one area of concern is the situation in the Ukraine. Although not big electronics industry players (Ukraine and Russia), the crisis could rattle markets around the world.

The sold-out show itself was very good; exhibitors were pretty happy. Their feelings were likely a direct result of the conference attendance, which translated into solid show-floor attendance. It will be interesting to see how it goes next year when we're back in San Diego.

Editor's Notes IPC APEX EXPO

by Lisa Lucke
MANAGING EDITOR, *THE PCB MAGAZINE*
CO-MANAGING EDITOR, *SMT MAGAZINE*

If you attended IPC APEX EXPO 2014 in Las Vegas last week, you'll know that it was a packed house for the most part, and offered something for everyone, from equipment on the show floor (many with "SOLD" signs) to technical conferences, standards meetings and of course, our *Real Time with...* video program. Our I-Connect007 team churned out more than 130 interviews with industry leaders, reps, fabricators, and designers, along with a handful of panel discussions that featured a moderated format aimed at generating lively discussion on key issues facing the industry, like onshoring, data file formats, the future of flex, and more. If you haven't seen it yet, check out our *Real Time with...* video index by clicking here. Most of the video interviews and panels are viewable now, and in the coming days, weeks and months, these videos will be featured in our newsletters and monthly magazines, and of course on our website. To subscribe to any of our publications, click here.

See you in San Diego in 2015!

Designers Step up at Design Forum

by Andy Shaughnessy
MANAGING EDITOR, *THE PCB DESIGN MAGAZINE*
CO-MANAGING EDITOR, *SMT MAGAZINE*

After two years in San Diego, the Design Forum was back on familiar turf this year as IPC APEX EXPO returned to Mandalay Bay Hotel and Convention Center in Las Vegas.

Forum speakers included Greg Munie of IPC, Karen McConnell of Northrop Grumman, Gary Carter of Fujitsu, Dieter Bergman of IPC, Mark Laing of Mentor Graphics, Humair Mandavia of Zuken USA, and Ben Jordan of Altium.

Although busy doing our *Real Time with...* video interviews much of the time, I managed to catch some of the sessions. Carter's discussion of the IPC-2581 data transfer standard was well received, and, of course, it led to some good back-and-forth during the Q&A period.

While sitting in on the Design Forum, Guest Editor Kelly Dack met first-time attendee Halil Yaslak, a PCB designer with Aselsan, a defense company in Ankara, Turkey. We talked him into doing a video interview. Yaslak was one of the younger designers at the Design Forum, but he's a heavy hitter; he took home first place honors at the 2012 Mentor Technology Awards for a 26-layer HDI board. He's definitely someone to watch and we look forward to seeing him next year if he's able to make the long journey again.

When the forum was over, most speakers and attendees trooped over to Rainer Thuringer's Professional Development class on optimizing high-speed design. Thuringer is chairman of the FED, a German organization that represents electronics designers and manufacturers. With a Ph.D. in physics, Thuringer has a unique viewpoint. He stresses the critical demand for finding "new blood," as well as the EMS community's need to focus upstream, on the challenges facing PCB designers and design engineers.

Altium's Ben Jordan also moderated our panel discussion on data transfer standards, which is always a contentious topic. As Ucamco's Karel Tavernier joked beforehand, "No daggers?" Tavernier's company owns the Gerber standard, and he joined Mentor's Dave Wiens, who represented

Designers Step up at Design Forum *Continues*

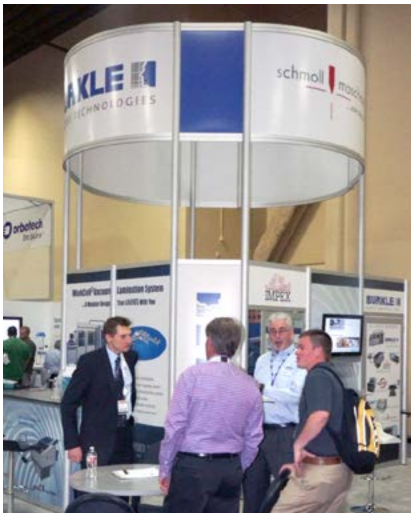
ODB++, and Hemant Shah of Cadence Design Systems, who is active in developing the IPC-2581 standard.

These panelists kept the marketing to a minimum and addressed the facts surrounding this hot-button issue. We shot a variety of these panels, but the data standard panel drew the biggest crowd; each format attracted its own entourage. But no panelists were injured during the filming of this panel.

In other news, Rick Hartley announced that he is really, truly retiring from L-3 Avionics this year. But he'll continue to teach design classes and stay active in the PCB community. He just won't have to get up to an alarm clock anymore, which sounds like a plan.

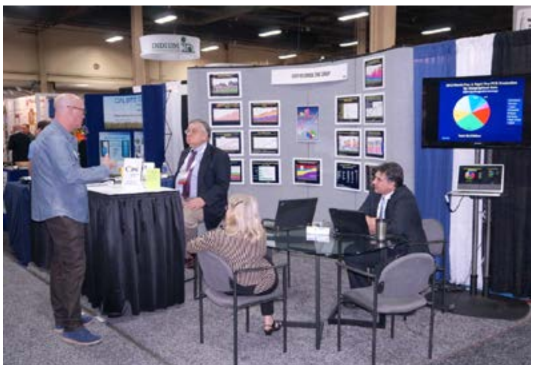
Overall, the Design Forum and IPC APEX EXPO went off without a hitch. Our booth was packed all week, with interviews set for every 15 minutes. And we saw solid traffic in the aisles the first two days, and OK traffic on the last day. Next year, the show moves back to (hopefully) sunny San Diego. See you in the Gaslamp Quarter!

Ben Jordan and Andy Shaughnessy

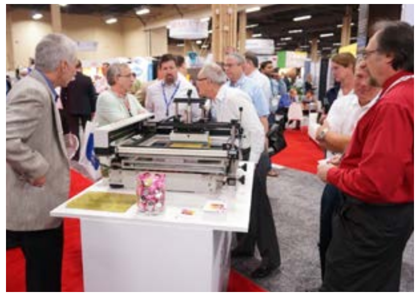


IPC APEX EXPO 2014
Show Review
LAS VEGAS, NEVADA

IPC APEX EXPO 2014 Show Review LAS VEGAS, NEVADA



IPC APEX EXPO 2014 Show Review LAS VEGAS, NEVADA



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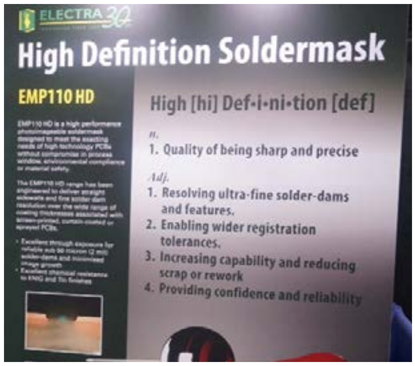
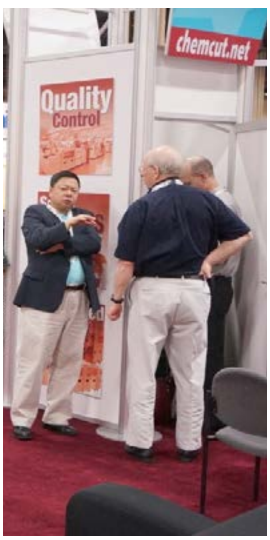
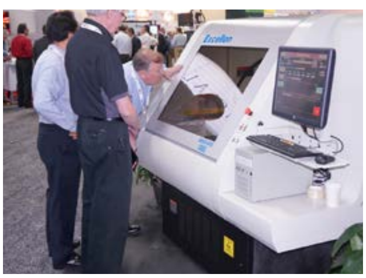






column

BROOKS' BITS

Electromagnetic Fields, Part 3: How They Impact Coupling

Douglas Brooks
ULTRACAD DESIGN

In the Part 1 and Part 2 of this series [1], I talked about how helpful it can be to recognize what the electromagnetic field looks like around a conductor or trace and how that field may change as we change the stackup or trace parameters. Visualizing how the electromagnetic field changes can give us insights as to how parameters like impedance and propagation speed might be influenced by the changes in the stackup or trace parameters. In Part 3, we will look at how changes in the electromagnetic field relate to changes in coupling between traces (crosstalk) or between a trace and the outside world (EMI).

(Special note: The figures in these three parts are largely taken from my new video lecture series just published by Prentice Hall, *PCB Signal Integrity LiveLessons*, and in particular from Lesson 1.4. Learn more about these LiveLessons at www.ultracad.com or at the Informit website.)

Let's begin the analysis by looking at Figure 1. It shows the electromagnetic field around an 8 mil microstrip trace that is 50 mils above the plane. It is separated from other traces by 50 mils. Note how the electromagnetic field extends way out into the air and over to other traces. This poses a significant possibility of EMI problems.

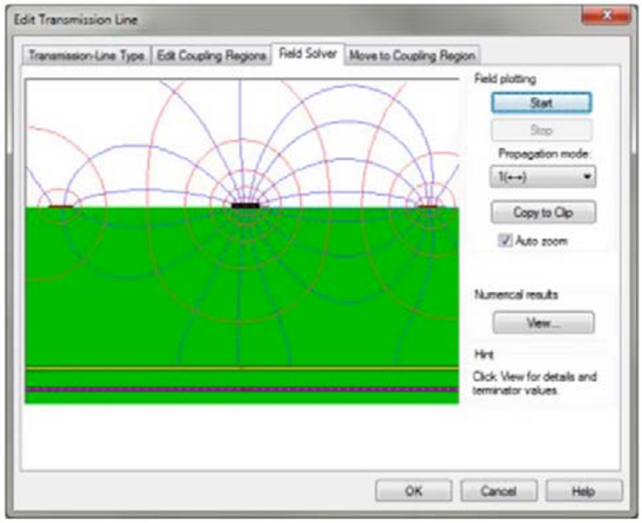


Figure 1: 8 mil trace, 50 mil height, 50 mil separation.

ELECTROMAGNETIC FIELDS, PART 3 *continues*

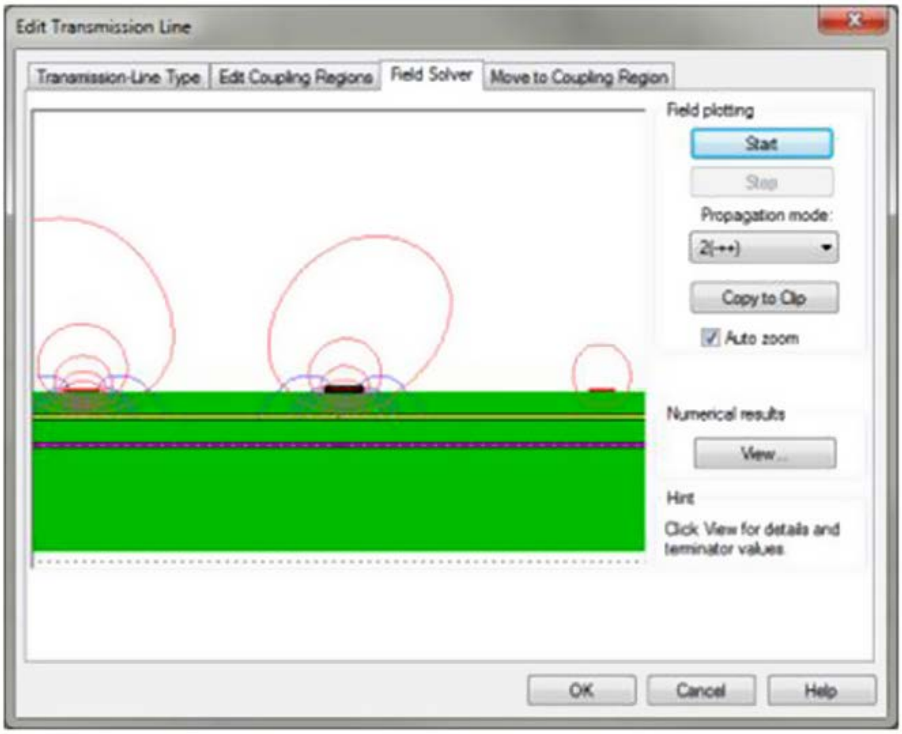


Figure 2: 8 mil trace, 5 mil height, 50 mil separation.

On the other hand, look at Figure 2. This shows the same three traces, but this time they are only 5 mils above the underlying plane. Now a substantial portion of the electromagnetic field is "captured" between the trace and the plane. This significantly reduces the potential for EMI radiation off the board. Simply by looking at the electromagnetic field we can intuitively see that this configuration will perform better from an EMI standpoint.

This graphically illustrates what is possibly the single most important design rule for signal integrity on PCBs:

Rule 1: Route every trace as close as practical to a continuous, related, underlying plane.

Next, let's look at Figures 3 and 4. They illustrate a pair of 8 mil traces, 5 mils above the plane, but in Figure 3 they are separated by 5 mils while in Figure 4 they are separated by 25 mils. When they are close together they couple into each other, raising the potential for crosstalk problems between them. But when we separate them the fields reduce their

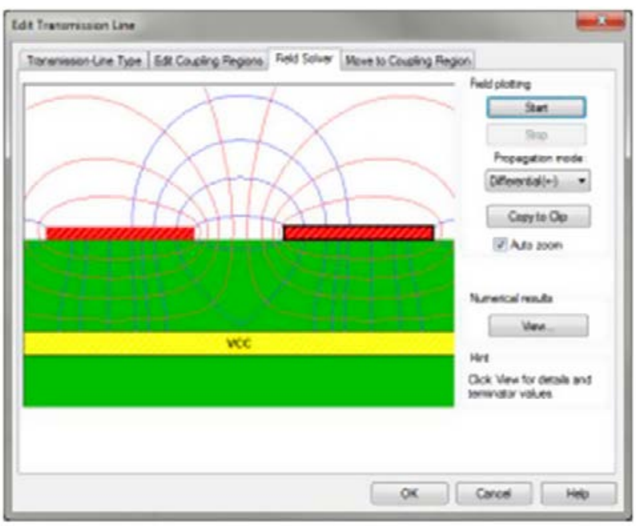


Figure 3: 8 mil traces, 5 mil height, 5 mil separation.

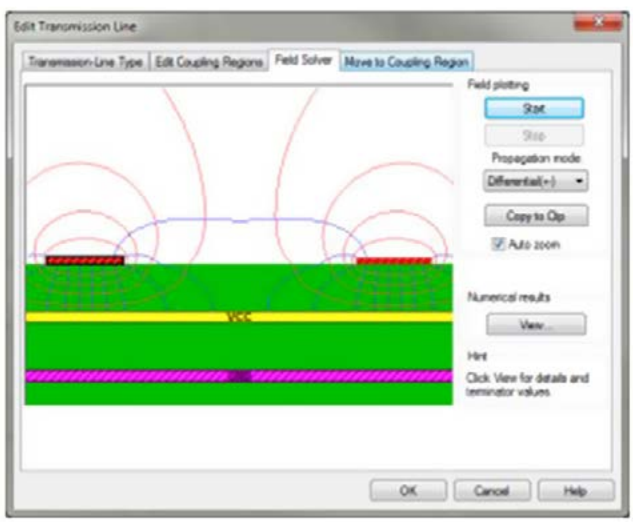


Figure 4: 8 mil traces, 5 mil height, 25 mil separation.

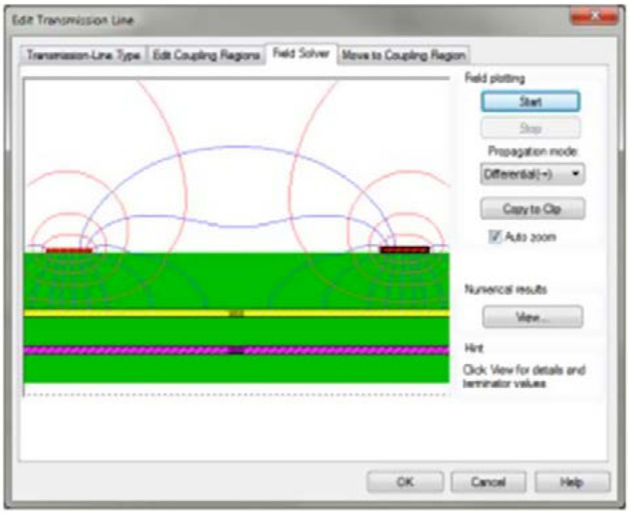


Figure 5: Microstrip 8 mil traces, 50 mil separation, 10 mil above plane.

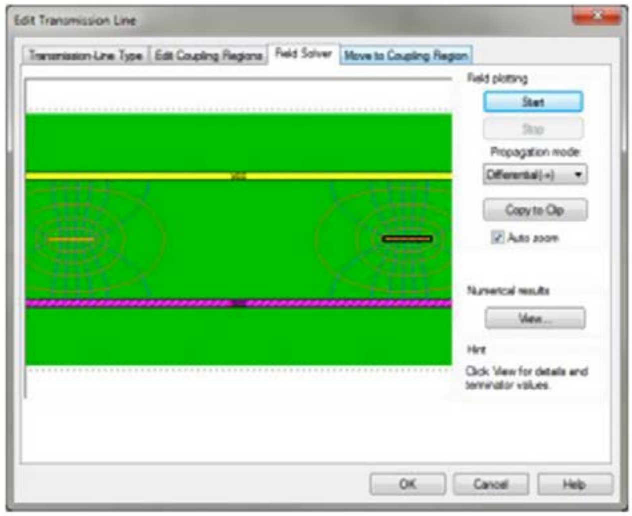


Figure 6: Stripline 8 mil traces, 50 mil separation, 20 mil between planes.

mutual coupling and the potential for crosstalk goes down.

We intuitively know that one solution for crosstalk is to separate the traces. By considering what the electromagnetic fields look like, we can see why.

Finally, look at Figures 5 and 6. They illustrate 8 mil traces with a 50 mil separation. In the microstrip case (Figure 5) the traces are 10 mils from the underlying plane. In the stripline case (Figure 6) the traces are 10 mils from either plane. Now however, in the stripline case, the electromagnetic fields are captured between the two planes. No part of the field is allowed to escape from between the planes. The fields are also restrained from spreading out as far as they do in the microstrip case. Clearly, then, the stripline case will perform better from both an EMI standpoint and a crosstalk standpoint.

It is tempting to draw the conclusion from Figures 5 and 6 that all critical traces should be placed in a stripline environment, and/or that good EMI performance can't be obtained in a microstrip environment. Be careful about this conclusion; it can be overstated. It is absolutely possible to design traces that perform perfectly well (from both an EMI and a crosstalk standpoint) in a microstrip environment. People do it all the time. Nevertheless, it is still true that the fields are contained better in a stripline environment.

These illustrations provide further evidence that by visualizing the electromagnetic fields around conductors or traces we can get an intuitive feel for how those traces will perform on an actual board from a signal integrity standpoint. **PCBDESIGN**

Notes

1. See How Electromagnetic Fields Determine Impedance, Part 1, and Electromagnetic Fields, Part 2: How They Impact Propagation Speed.

Douglas Brooks, PhD, is the founder of UltraCAD Design and now retired from daily work. He has written numerous articles in several disciplines and has held signal integrity seminars around the world. Brooks has spent most of his career in the electronics industry in positions of engineering, marketing, management, and as CEO of several companies. Prentice Hall has recently published his latest book, PCB Currents; How They Flow, How They React, and a seven-hour educational video series on signal integrity. Visit his website at www.ultracad.com.

The Internet of Things Drives New PCB Design Approach

by Mark Toth
CADSOFT COMPUTER

This article originally ran in the February issue of *The PCB Magazine.*

The most common question asked of electronic product developers today is how to do more with less. How do you incorporate newer, faster technologies in smaller packages to take advantage of new products and architectures that provide more functionality and power efficiency, all on time and under budget? Is it possible to retool processes without negatively impacting designer productivity? Can advanced techniques and current best practices be made available at the designer's fingertips during development, without leaving the design environment?

Increased consumerization of electronics and a convergence of various elements of functionality, due in part to the Internet of Things (IoT), are putting intense economic pressure not only on time-to-market, but on cost of development as well. Add to that increased competition in the electronics industry and continued globalization, and we're seeing increased investments in tools, training, new best practices and increasing openness to collaboration.

To illustrate the continued globalization, according to information released by the EDA Consortium in an October press release, PCB and multi-chip module revenue is at $148.3 million, a YoY increase of 5.2% compared to the same quarter in 2012. The four-quarter moving average for PCB and MCM, however, increased 10%. This is compared to overall industry revenue which increased only 3.8% YoY for the same quarter reported, but dropped almost 1% in sequential quarters. The four-quarters moving average, which compares the most recent four quarters to the prior four quarters, increased by only 5.3%.

Not surprising, a geographic trend for the design tool industry shows revenue for all design tools in the Asia-Pacific region increased

to $431.9 million in the most recent quarter reported, an increase of 18% compared to the same quarter of the prior year. The four-quarter moving average increased 14.4%.

The financial opportunity for electronic product development is exponential, but there are major pitfalls as well. A simple rule of thumb in management consulting practices states that, on average, companies lose a third of after-tax profit when they ship products six months late. One could easily argue the penalties are significantly greater in the consumer electronics market, which has now far exceeded the $200B mark.

Design cycle time plays a big part in determining a product launch schedule, and the PCB layout part of this process is often called upon to make up for early design phase schedule slips. In today's competitive climate, finding ways to reduce design cycle times is a priority for all engineers. Of chief concern for many companies is that as PCB design becomes more and more complex, engineers need to have cost-effective tools that reduce time-to-market. Another potential challenge is the fact that companies have design teams dispersed all over the world.

Given all those factors, it's easy to see how completing a product launch within the specified time frame can be daunting. To address all of these challenges, companies need tools that can leverage their existing resources (both human and computer), allow interoperability, have a gentle learning curve and can offer extensions that link other time-intensive parts of the design cycle or supply chain.

In a recent industry survey conducted by CadSoft Computer, designers from 42 different countries weighed in on future requirements, as well as emerging trends in electronic product development.

Some of the results were surprising:

- Sixty-four percent of respondents think development boards are reducing the need for custom PCB design
- Almost half (46%) are developing with open source hardware platforms
- Eighty-three percent agree peer-to-peer communities are important, while 25% believe they are essential

Other results were not unexpected:

- The majority of designers put functionality before cost when buying design tools, with 60% of respondents rating functionality as an "extremely important" factor
- A design tool should offer a gentle learning curve

Design tools should:

- Allow multiple designers to lay out a single project without sacrificing productivity
- Have a plug-and-play model for tasks that are intensive to increase productivity
- Allow designers to collaborate with each other in real-time from anywhere in the world

While it is true that more and more design projects are being started with off-the-shelf development kits and boards instead of designing a PCB from scratch, engineers will often need to design an interface board (such as a shield, cape, expansion, daughter card, etc.). This is a market where many PCB tool companies, including CadSoft, have significantly benefited.

As more and more open source hardware platforms are finding their way into commercial development projects, some large global silicon suppliers are now offering such low-cost open source kits to the maker and hobbyist in hopes of increasing demand for their technologies. TI's Launchpad series is just one example.

What about peer-to-peer, social media, designing in the cloud and other forms of collaboration? Are these trends fuelling designer productivity?

Although somewhere between novel idea and trend, a few considerations need to be addressed before the cloud is deemed mainstream for electronics design. These considerations include risk and compliance (such as data security and retrieval), flexibility (access and control) and timing (different services will benefit from moving to the cloud sooner). From a business standpoint, it is more likely

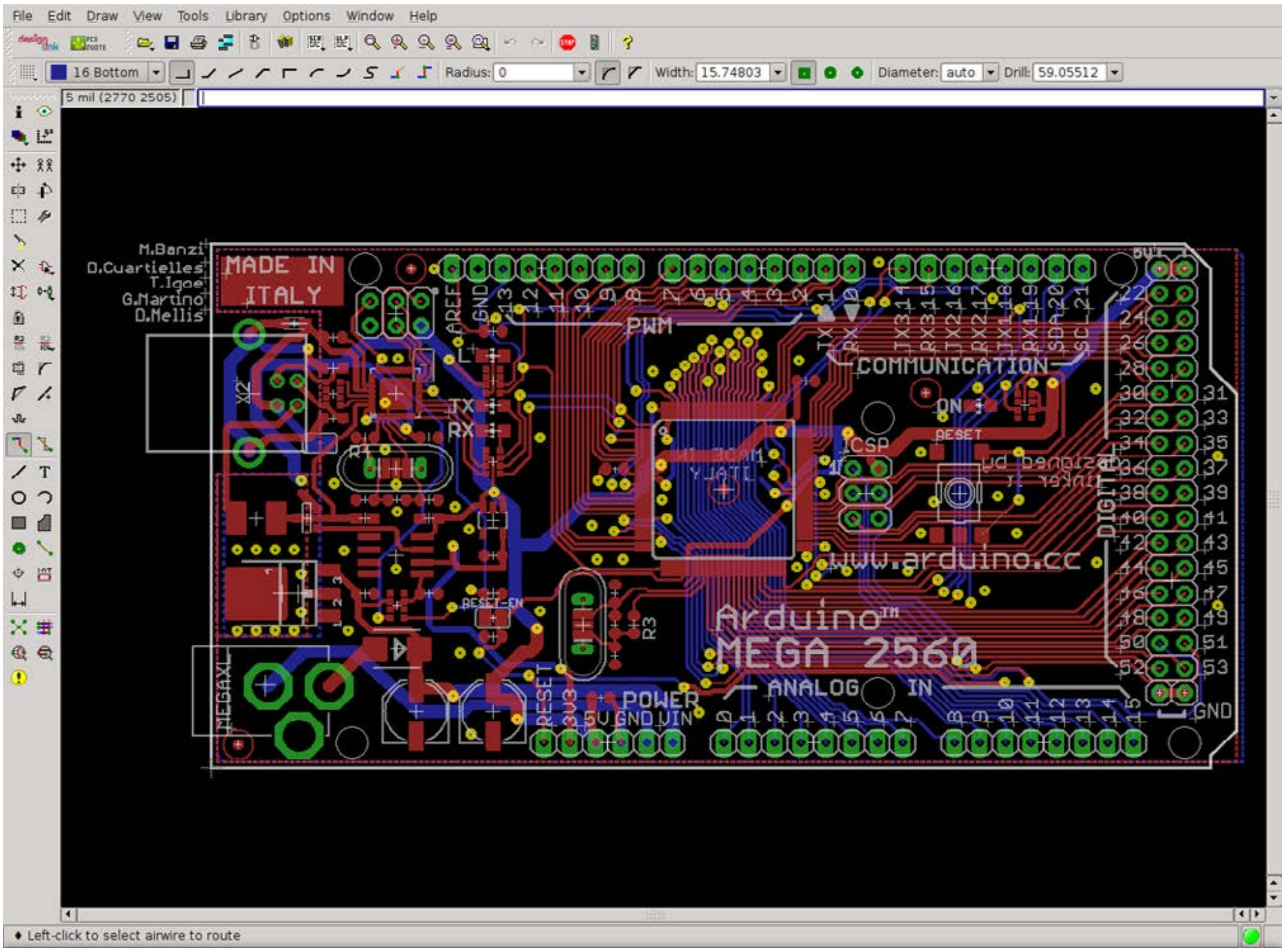


Figure 1: The Arduino Mega 2560 reference design and schematic in CadSoft EAGLE.

to occur in PCB design first, as there are so many more PCB designers to make it a more sustainable model. Determining factors for a design application to harness the power of the cloud are tied to obvious benefits such as increased speed and capacity, lower cost, security and so on. If your design application is not performance-intensive, or the cloud does not lower your development costs or improve productivity, it might not make sense just yet.

Other online resources and communities, however, have existed for years helping engineers get answers, find common design elements and identify new technologies faster. Element14.com, the first and largest online engineering community with more than 200,000 members, enables developers to connect with like-minded peers to gain design inspiration or obtain expert answers and opinions. One of its most active forums is hosted by the CadSoft EAGLE user community. In addition to answers and advice, element14 contains a free database of CAD libraries, which are searchable by component supplier, thus enhancing designer productivity and cost to develop.

Another trend that continues to evolve in the PCB design industry is tighter forms of integration between electrical and physical design. To efficiently bring a new product into production, electrical CAD (ECAD) and mechanical CAD (MCAD) data must be merged. A virtual 3D representation of the PCB geometry within MCAD tools allows mechanical engineers to quickly design product housings as well as other mechanical features that fully utilize the available 3D real estate. MCAD features such as cross-section views and interference checks help ensure that there will not be any future fit issues when prototypes are built.

Keith Richman, president of Simplified Solutions, said:

Generating a virtual 3D representation of PCB geometry within MCAD tools has historically been a time consuming task. Intermediate Data Format (IDF) has been around for 20+ years, but in the earlier days of IDF, the labor involved to create 3D PCB representations was time consuming and costly. In 2014, many tools are available to help expedite the 3D PCB process. Manufacturers and online services now provide 3D STEP models that can help populate a 3D PCB. In addition, some solutions contain integrated 3D component libraries that allow the 3D geometry task to be completed in just hours. 3D printer technology can then be utilized to generate a geometric 3D representation of PCB geometry prior to the more expensive manufacture of PCB prototypes.

Speaking of component libraries, the amount of information needed on thousands of different components threatens to overwhelm even the most organised professional. A challenge for board designers with this sort

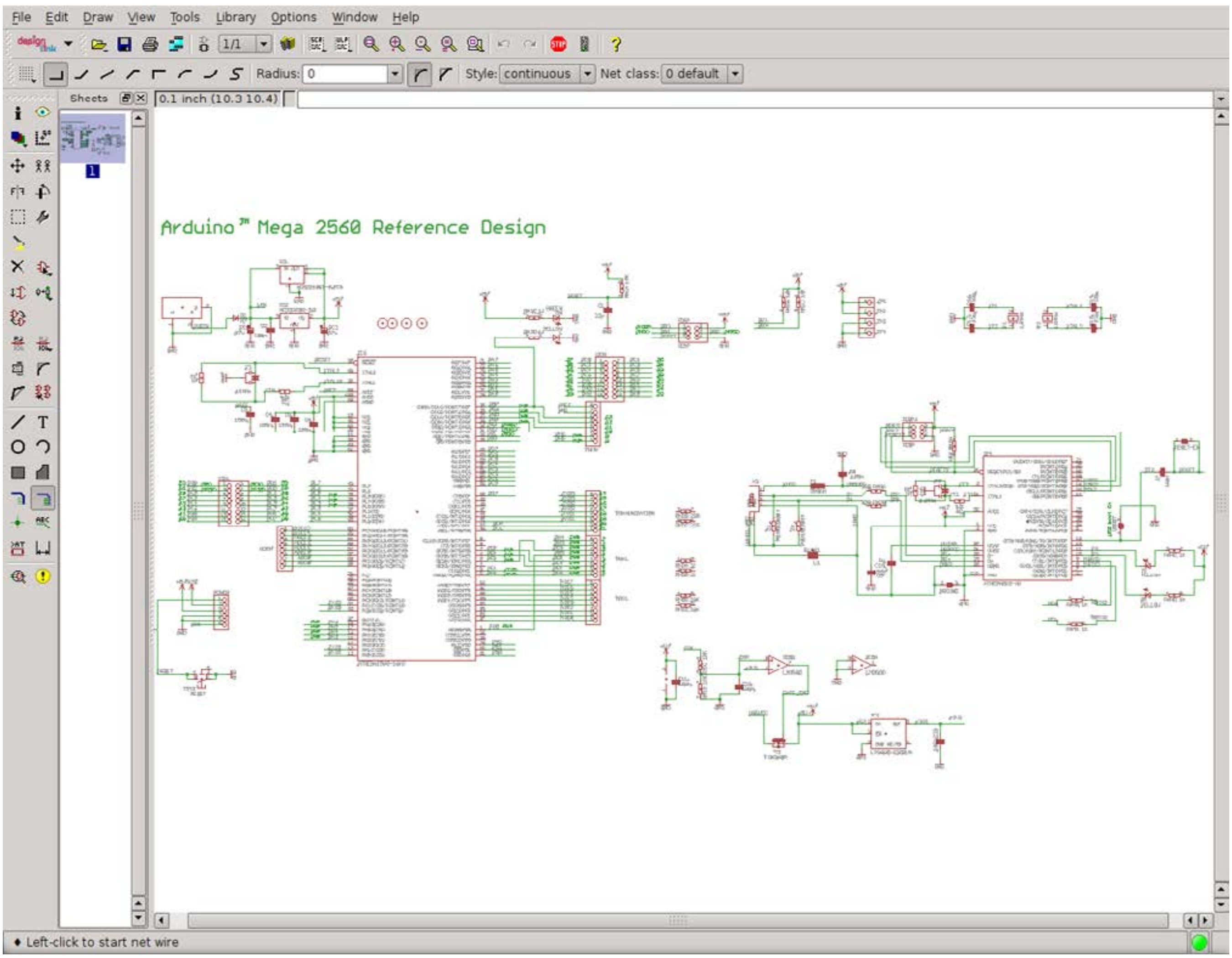


Figure 2: Schematic of the Arduino Mega 2560 reference design.

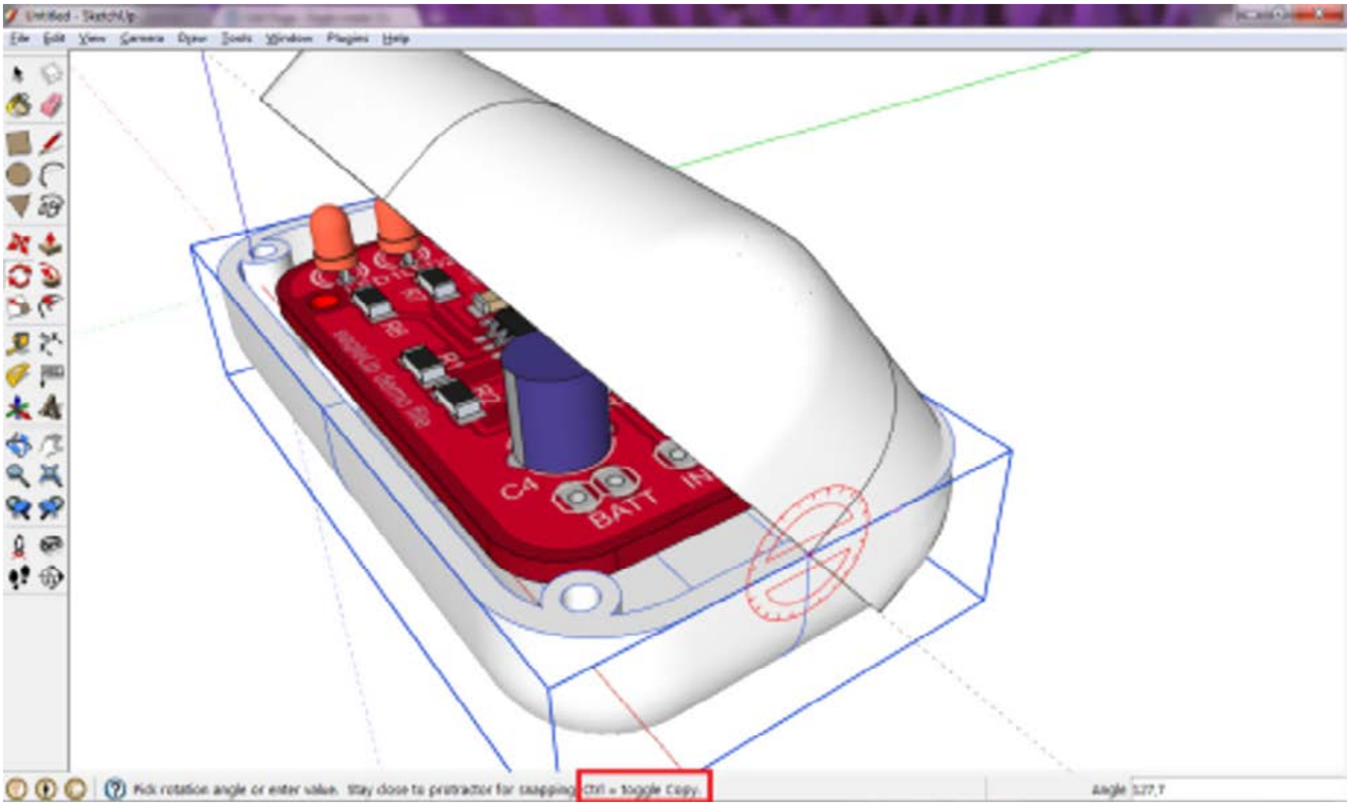


Figure 3: 3D visualisation enables users to simulate larger systems, here shown as a PCB board design in an enclosure. This saves time and cost even before prototype is built. (Source: EagleUp)

of technology is dealing with and creating the complex shapes needed to implement the components. Engineers regularly mention spending too much precious product development time creating footprints or in other parts of library management. This is a very important issue. You can't be designing a custom part for each component you want to add to your circuit.

While some third-party tools come with many libraries already, tens of thousands more are available online or in design portals from manufacturers and user shared libraries such as the element14 community. Building a custom library from scratch can take over 20 minutes per part for a small quantity, so being able to rely upon a rich pool of information validated by an active community is a significant benefit. Within complex devices, if the design is open users can specify the parts through an integrated search on a parts database with an online distributor or electronics supplier. This allows electronic design engineers to immediately search and find parts online with parametric search to choose the right components, and they have access to a huge amount of technical information regarding the components themselves. This includes technical datasheets, links to guidance on solutions for specific applications, pricing and availability. This "virtual integration" of the design chain not only enhances design quality and designer productivity, but it reduces risks associated with misidentifying a critical component or selecting a part that is obsolete or out of stock.

Jeremy Blum, open hardware designer and hardware engineer at Google, points out:

As designs continue to get more and more complex, following best practices becomes more and more important. For novice designers, it's easy to encounter a myriad of potential design problems that may or may not be caught by traditional DFM checks. Some of the things to look for when preparing a PCB for production are problems that are *only fully understood by designers who have been doing PCB CAD for many years. Luckily, as open source designs become more common place, and as more and more professional designers join communities like element14, it becomes easier and easier for new designers to get help and tips from industry veterans. A truly community-driven design platform makes the barriers to entry lower than ever before.*

Once engineers have honed in on the bill of materials that fits the project budget and are ready to fabricate the PCB, very often one has to send it off and wait. Users should be able to access instant quotations for their small volume PCB fabrication and take advantage of quick-turn prototyping service from reliable, high-quality service partners through a one-click integrated "PCB quote" link.

Prototyping is as much about mechanical fit and manufacturability as it is about functionality, quality and performance. Designers are packing more and more components onto smaller and smaller boards into smaller enclosures, placing unprecedented demands on design, analysis and simulation tools.

Ed McMahon, CEO of Epec Engineered Technologies:

Many are resorting to exotic and/or aluminium-clad PCB materials that are blind/buried via technology to fit all of the required functionality onto their circuit boards. Choose a design solution that not only easily places those features into your design, but also allows you to clearly and accurately communicate to your PCB fabricator what you are trying to accomplish. Many design products allow you to use the features and test them in your design, but do not give the fabricator the specific data they need to manufacture the product.

While there are a plethora of commercial products available (most of them expensive to very expensive), there are relatively few that are low cost and lend themselves to the notion of "virtual design chain integration." For whichever path you choose, it is important to weigh factors such as openness and capacity for integration, ease of use, flexibility and community affiliation. It is this ease-of-use that is increasingly becoming important to balance how complex design can be accelerated while keeping the upfront design costs low.

Despite the increasing levels of semiconductor integration and readily available systems-on-chips for many applications, not to mention the increasing availability of highly-featured development boards which can be used out-of-the-box, electronics product development in many cases still relies heavily on custom PCB design. Even for one-off developments, the humble PCB still performs an important role; it's a physical platform for your design and it's also the most flexible ingredient to pull any electronics system together. PCBDESIGN

Mark Toth is the business development manager at CadSoft Computer.

NASA's Latest Satellite Phones Home

PhoneSat 2.4 has phoned home. The tiny spacecraft that uses an off-the-shelf smartphone for a brain has completed checkout and sent back data confirming all systems are "go" for the spry spacefarer.

PhoneSat 2.4, a cube approximately four inches square, weighs only about 2.2 pounds, and was developed at NASA's Ames Research Center in Moffett Field, California. It is confirming the viability of using smartphones and other commercially available electronics in satellites destined for low-Earth orbit.

Data from the satellite's subsystems, including the smartphone, the power system and orientation control system are being downlinked over amateur radio at a frequency of 437.425MHz.

Mil/Aero007 News Highlights

Ducommun Gains TOW Missiles Contract from Raytheon

Ducommun Incorporated has received a follow-on award from Raytheon Company to continue providing complex wiring harnesses and printed circuit card assemblies for the tube-launched, optically-tracked, wireless-guided (TOW) weapon system. The contract extends the Company's support of the program through 2014.

Nortech's 17% Sales Rise Driven by New Programs

Nortech Systems Incorporated, a leading provider of full-service EMS, has reported net sales of $29.3 million for the fourth quarter ended December 31, 2013, a 17% increase compared with net sales of $25 million for the fourth quarter of 2012.

MC Assembly Achieves AS 9100 Rev C Certification

This certification, which provides a common set of quality requirements across the global aerospace community, accredits MC Assembly's Quality Management System compliance to the aerospace requirements to manufacture and service PCB assemblies, sub-assemblies, and final assemblies.

Sypris' Electronics Group Posts 20% Revenue Drop

Revenue for the Electronics Group was $10 million in the fourth quarter of 2013 compared to $12 million in the prior year period, reflecting lower product sales to overseas customers and budgetary and funding uncertainties within the U.S. DoD.

MINT Region to Increase Defense Spending by $20B

ReportsnReports.com adds "Future of the MINT Defense Industry—Market Attractiveness, Competitive Landscape and Forecasts to 2019" research report to its store. It says the MINT defense industry is expected to become one of the most attractive defense markets in review period. The Mexico, Indonesia, Nigeria, and Turkey (MINT) region is expected to increase its defense spending from US $40.6 billion to US $61.1 billion over the forecast period, according the new report.

Orbit Reports Sales Drop in Q4, FY 2013

Mitchell Binder, president and CEO, stated, "2013 was a difficult year for our company resulting from challenging business conditions in the defense industry. Like most companies in our industry, including large defense prime contractors, as well as short sales cycle defense contractors like Orbit, our revenues declined from the prior year as reorders on many of our legacy products were delayed..."

Advantage Eyes Special Nuclear Materials Project

In a recent statement, President and CEO Jody Singleton declared, "Advantage will be honored if awarded a contract and we will be proud to bring our unique capabilities in gamma spectroscopy threat detection as well as the benefits of the small size, light weight and exceptional power management features we typically employ in instrumentation development.

Military Communications Market to Reach $30B by 2022

"Managing bandwidth in increasingly congested spectrum will be a key challenge in meeting future demands for data-centric military communications," observed Asif Anwar, director of the ADS service. "This is leading to the use of higher frequencies, particularly evident in the military satellite communications segment with adoption of Ka-band."

DoD Releases 2015 Budget Proposal of $495.6 Billion

President Obama has sent Congress a proposed defense budget of $495.6 billion in discretionary budget authority to fund base defense programs in fiscal year 2015. The request is $0.4 billion less than the enacted FY 2014 appropriation and is consistent with the current budget caps.

India Becomes Largest Defense Market for U.S.

"We are seeing trade patterns fundamentally change for the dominant players," said Ben Moores, the study's author. "The most notable change is the spectacular level of imports from India. China, Indonesia, Egypt, and Taiwan all saw imports increase by one billion. When we look at India, those figures were $5.9 billion. By 2015, our forecasts show that number jumping to $8.16 billion."

Hybrid High-Frequency Multilayer PCBs

by John Coonrod
ROGERS CORPORATION

A hybrid multilayer PCB uses materials with significantly different critical properties than those associated with a traditional multilayer PCB. A hybrid could use a mix of FR-4 materials with high-frequency materials, or a mix of different high-frequency materials with different dielectric constants. Hybrid construction is becoming more popular as technology evolves, but they bring with them some benefits and challenges which need to be better understood.

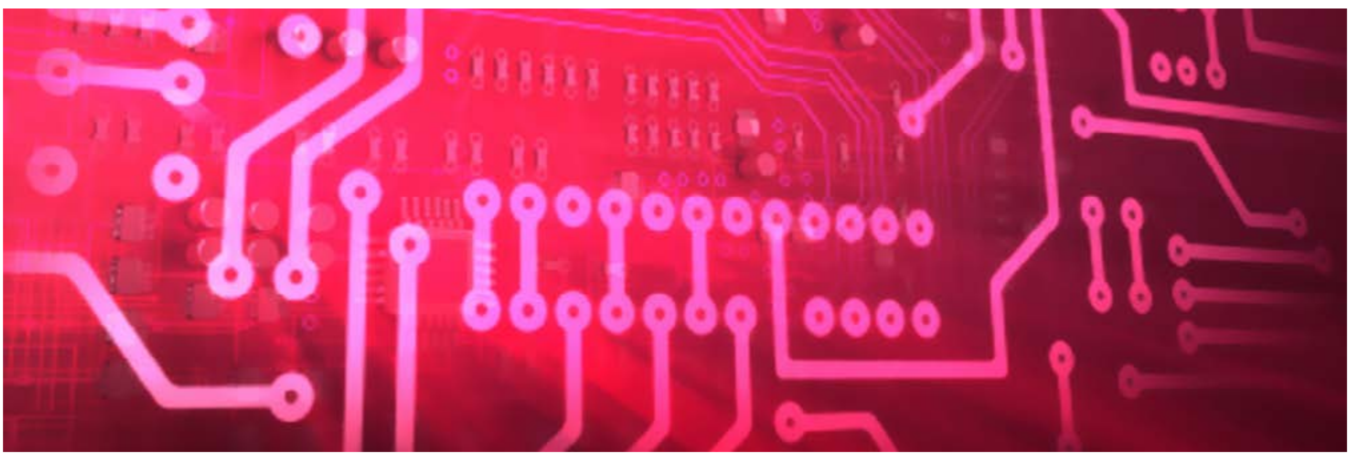
The reasons for using a hybrid multilayer PCB typically fall into one of three categories: cost, improved reliability, or enhanced electrical performance. High-frequency circuit materials are typically more expensive than FR-4 types. Sometimes, hybrids using a combination of these two different materials are constructed to ease cost issues. Many times, a multilayer PCB will feature some circuit layers that are electrically critical and many layers that are not critical. In this case, the less expensive FR-4 material is used in the non-electrically-critical layers and the more expensive high-frequency material is used in the more critical layers.

Another reason for using hybrid multilayers is to improve reliability when one of these materials has a high CTE. Some high-frequency PTFE materials have high CTE properties and that can be a reliability concern. When an FR-4 material with a low CTE is used in conjunction with the high CTE material to make the multilayer, the composite CTE can be acceptable.

Some hybrids use materials with very different dielectric constants that are used for enhanced electrical performance. In the case of some couplers or filters, it may be advantageous to use laminates with different dielectric constant values.

The combination of FR-4 and high-frequency materials is becoming more common since there are few compatibility issues related to using FR-4 and most high-frequency circuits materials. However, there are several circuit fabrication issues which need to be understood.

The type of high-frequency material used in a hybrid construction can make a big difference in the degree of special processing needed for circuit fabrication. PTFE-based high-frequency materials can be more problematic for circuit fabrication due to special drilling and plated through-hole (PTH) preparation requirements. Hydrocarbon-based laminates can easily be fabricated using standard FR-4 circuit board processing techniques.



A combination of FR-4 materials and high-frequency hydrocarbon laminates typically has few circuit fabrication issues. The main concern with this combination of materials is typically drilling and lamination. A DOE (design of experiments) is usually necessary to establish the proper feeds/speeds for drilling a circuit of this combination of materials. Lamination can be an issue for FR-4 prepreg, which often requires a ramp rate that is very different than the high-frequency prepreg. In order to make a more reliable hybrid, there are a couple of options to consider when using FR-4 and hydrocarbon prepreg. One option is to replace the FR-4 prepreg with the high-frequency prepreg and use the appropriate lamination cycle. A high-frequency prepreg is typically not as expensive as the laminate, and having all bonding layers made of the same material is beneficial for a simpler lamination cycle. When the FR-4 prepreg cannot be replaced, it may be necessary to do sequential lamination, where the first lamination cycle cures the FR-4 prepreg and the second lamination cycle cures the high-frequency prepreg.

"A high-frequency prepreg is typically not as expensive as the laminate, and having all bonding layers made of the same material is beneficial for a simpler lamination cycle."

A hybrid multilayer PCB using a combination of FR-4 and high-frequency PTFE circuit materials can be more challenging, however there are some exceptions. There are several different types of PTFE-based laminates and some are easier to fabricate than others. Even though ceramic-filled PTFE-based laminates have less circuit fabrication concerns than a pure PTFE laminate, drilling, PTH preparation and dimensional stability must be considered.

The main concern about PTH drilling is that the PTFE material is relatively soft and the FR-4 material is rigid. When the PTH is drilled and the drill tool goes through the interface of these material boundaries, the hole can have a flap of soft material stretched over some length within the PTH wall. This can be a serious reliability issue and must be addressed. Typically the proper feeds and speeds must be determined through a DOE and a study regarding drill life. Many times the flap defect does not occur early in the drill tool life, so understanding the drill life is important for minimizing this concern.

The PTH preparation must address both types of materials for the plated through-hole process. The plasma cycle will probably need to be two different cycles or one cycle with multiple stages. The FR-4 materials should be treated in the first plasma cycle and the PTFE materials in the second cycle. Typically, the plasma process for FR-4 uses CF_4-N_2-O_2 gases, and PTFE uses He or N_2H_2. For improved through-hole wall wettability, the recommended cycle using helium (He) is a better choice for treating PTFE. If wet processing is used to prepare the PTH, perform the permanganate first for the FR-4 materials followed by sodium naphthalene to treat the PTFE material.

Dimensional stability or scaling can be an issue with PTFE and FR-4 hybrids. This can be reduced by minimizing mechanical stress of the PTFE laminate. Scrubbing the panel induces random mechanical stresses and is not recommended. A chemical clean process is a better method for preparing the copper for subsequent processing. The thicker PTFE laminates will have less issue with dimensional stability and the woven-glass reinforced PTFE substrates will be more stable as well.

In general, the manufacture of hybrid PCBs with a combination of FR-4 and high-frequency circuit materials has few compatibility issues. But several circuit fabrication concerns need to be addressed. When working on hybrid multilayer builds, it is always recommended that the fabricator consult with the material manufacturer for best results. **PCBDESIGN**

John Coonrod is a market development engineer for Rogers Corporation, Advanced Circuit Materials Division. To reach Coonrod, click here.

video interview

Intercept Adds Capabilities to Pantheon

by Real Time with...
The Design Forum

Dale Hanzelka, North American sales manager for Intercept Technology, discusses a variety of new features that have been added to the Pantheon design tool suite.

CLICK TO VIEW

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Quantum Photon Properties Revealed in Another Particle

For years, researchers have been interested in developing quantum computers—the theoretical next generation of technology that will outperform conventional computers. Instead of holding data in bits, the digital units used by computers today, quantum computers store information in units called "qubits." One approach for computing with qubits relies on the creation of two single photons that interfere with one another in a device called a waveguide. Results from a recent applied science study at Caltech support the idea that waveguides coupled with another quantum particle, the surface plasmon, could also become an important piece of the quantum computing puzzle.

The work was published in the print version of the journal Nature Photonics.

As their name suggests, surface plasmons exist on a surface--in this case the surface of a metal, at the point where the metal meets the air.

"If you imagine the surface of a metal is like a sea of electrons, then surface plasmons are the ripples or waves on this sea," says graduate student Jim Fakonas, first author on the study.

However, the plasmon's odd behavior, which falls somewhere between that of an electron and that of a photon, makes it difficult to characterize.

Because plasmons are very lossy--that is, easily absorbed into materials that surround them--the path is kept short, contained within a 10-micron-square chip, which reduces absorption along the way.

Indeed, the experiment confirmed that two indistinguishable photons can be converted into two indistinguishable surface plasmons that, like photons, display quantum interference.

TOP TEN

News Highlights from PCBDesign007 this Month

① Complete IPC Designers Forum Coverage From Las Vegas

The Designers Forum is now over, but we have in-depth interviews with the movers and shakers of the PCB design world. If you couldn't make it to Las Vegas, don't worry—we've got you covered!

② Mentor Solution Links PCB Design and Manufacturing

Mentor Graphics Corporation has announced its unique new product introduction (NPI) solution that seamlessly links printed circuit board (PCB) design and manufacturing operations to deliver the industry's first integrated, automated flow for the design, fabrication, and assembly of PCBs.

③ Zuken Launches CR-8000 Design Gateway, Design Force 2014

For high-speed designs, topology templates can now be created based on reference designs that include guidelines for track lengths, widths, and spacing—greatly reducing the effort to configure and manage constraints, especially with differential pair routing.

④ Douglas Brooks' New Book Explains Current & SI Issues

"PCB Currents: How They Flow, How They React" is aimed at helping PCB designers and fabricators better understand the conditions that lead to signal integrity issues on printed circuit boards, and how to control those issues. It is available in both a hard-bound and enhanced eBook version.

5 Bay Area Circuits Introduces Web-based InstantDFM Tool

Bay Area Circuits, Inc., a leading manufacturer of quick-turn PCBs, has announced the release of a new DFM tool named InstantDFM. This first-of-its-kind, fully automated, web-based tool enables PCB designers all over the world with the ability to upload their Gerber files and immediately receive a design for manufacturability (DFM) report.

6 Altium Partners with Octopart for Altium Designer

Altium Limited announces a third-party developer partnership with Octopart, a well known provider of an electronic parts search engine used by hundreds of thousands of engineers to find and compare parts across different manufacturers and distributors.

7 EMA Launches TimingDesigner 9.4 for DDRx Sign-off

"This integration allows the Sigrity solution to automatically export cycle-accurate timing simulation results to TimingDesigner for graphical viewing and analysis," said Manny Marcano, president and CEO. "This is the only solution on the market which combines power-aware sign-off-level simulation accuracy with fully parameterized timing diagrams to ensure DDRx sign-off success."

8 Sunstone Unveils PCBExpress Quickturn Quote Form

"Our PCBExpress Quickturn service is designed for those customers who need their PCBs quickly, for their time-sensitive projects," said Sunstone's CEO Terry Heilman. "With the new Quickturn Quote Form, we've eliminated the guesswork, and made the quoting process even faster and more efficient."

9 51st DAC Opens Registration; Announces Tech Program

The Design Automation Conference (DAC) is pleased to announce the technical program for 2014. The program consists of an exceptional quality of papers, panels, special sessions, keynotes, SKY Talks, Designer Track presentations, Work In Progress (WIP), workshops, full day tutorials, and training. New to the program in 2014 are three special initiatives focused on automotive, IP design, and security.

10 EDA Consortium Reports 5.7% evenue Growth for 4Q13

Printed circuit board and multi-chip module (PCB & MCM) revenue of $190.8 million represents an increase of 14.2% compared to Q4 2012. The four-quarters moving average for PCB & MCM increased 6.6%.

events

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For a complete listing, check out *The PCB Design Magazine's* event calendar.

Intermountain (Boise) Expo & Tech Forum
April 17, 2014
Boise, Idaho, USA

Smart Fabrics & Wearable Technology 2014
April 23–25, 2014
San Francisco, California, USA

NEPCON China 2014
April 23–25, 2014
Shanghai, China

Nordic SI Week 2014
May 5–9, 2014
Stockholm, Sweden

Atlanta 18th Annual Expo and Designers' Roundtable
May 7, 2014
Duluth, Georgia, USA

International Conference on Soldering and Reliabilit
May 13–15, 2014
Toronto, Ontario, Canada

Toronto SMTA Expo & Tech Forum
May 15, 2014
Toronto, Ontario, Canada

12th Annual MEPTEC MEMS Technology Symposium
May 22, 2014
San Jose, California, USA

51st Design Automation Conference
June 1–5, 2014
San Francisco, California, USA

IEEE MTT International Microwave Symposium
June 1–6, 2014
Tampa Bay, Florida, USA

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May:
Design For Manufacturing

June:
Designing Flex Circuits

July:
Concurrent Design